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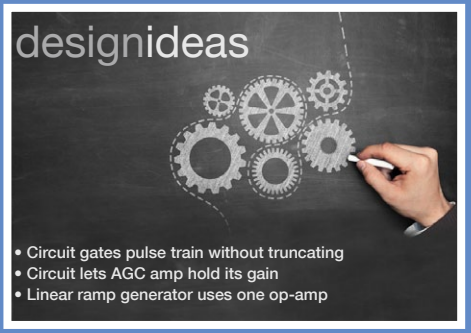

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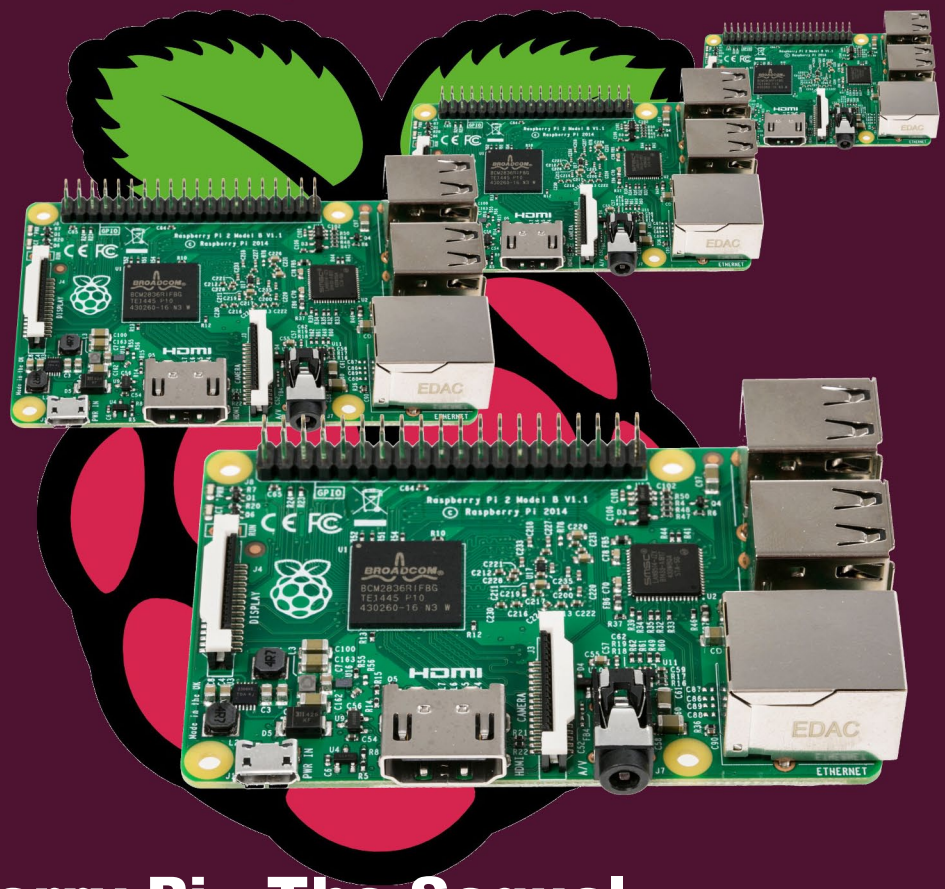
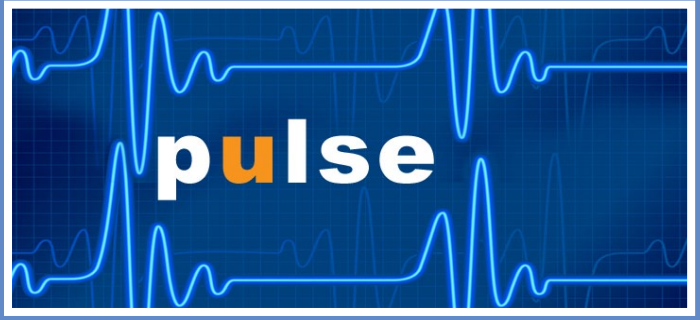
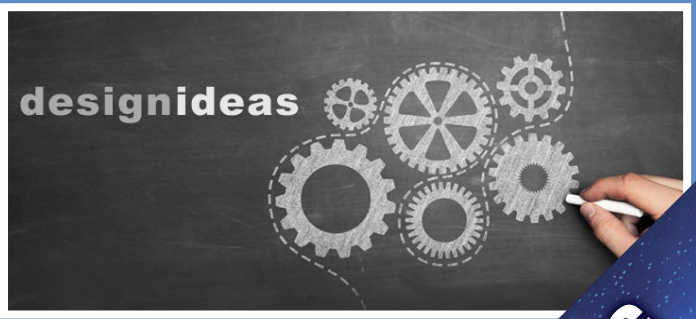


Raspberry Pi - The Sequel





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COVER

Raspberry Pi 2 steps up to 4-core CPU, doubles memory, still for $35

By some margin the most popular item in our pages this month has been the introduction of the second-generation Raspberry Pi computer board. It is now three years since the debut of the first Raspberry Pi, in which time it has sold over 4.5 million units, in a number of guises. In terms of sales volume, say its makers, it has "continued to surprise". When first put into production they thought it might sell 10 or 20,000 units in its first year; a spokesman for one of its distributors RS Components recalled that they first listed it with some caution, only to have the volume of orders stress RS' website.

Much was made initially of its role in education, where it has become something of cult item. In those three years, its applications have spread far beyond that space: as well as pervading the "maker" domain, it has now become a widely-used computing unit in many embedded control and supervisory functions. Read more on page 6, and from the two linked items there.

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HOW "OFF" IS "OFF"?

I recently spoke with Senior VP of power supply maker CUI, Mark Adams, on the subject of new mandates for energy efficiency that will be required of external "adaptor"-style equipment power supplies. CUI thinks that the market – that's you – isn't sufficiently aware of some fairly imminent changes that affect, in this instance, equipment sold into the US market. Imminent, that is, in terms of getting a supply chain organised and stocked, and any necessary design changes made, by the key date, which is February 2016.

We'll come back to this topic but, briefly, the parameters of this shift are; it applies to equipment for sale in the US; it relates only to adaptor supplies; and it focusses on standby power levels. The change is to the "Level VI" (these things are denoted in Roman numerals) specification and in the case of the US marks a significant shift because the legislation there is stepping directly from Level IV to Level VI. The change also brings into scope more powerful (to 250W) external supplies than prior regulations encompassed. There's an algorithm, but broadly, think in terms of 500 mW standby having to drop to 100 mW. Naturally, CUI would like you to know that they saw this coming and can sell you compliant hardware very soon.

So far, so green; there is of course the usual calculation that takes standby power levels of such devices, multiplies them up assuming they are all left connected when inactive, and renders the results in the metric of numbers-of-power-stations of wasted supply. And, by extension, the reduction in that figure of waste, that the legislation can claim to have achieved – or will achieve. I have never been entirely convinced of the validity of those calculations, although the basic principle is sound. They are somewhat latitude-dependent; standby dissipation is especially wasteful when it happens in an air-conditioned environment but here at 52degrees north, I have to heat my home for about 7 months of the year and my devices in standby are mostly just contributing a (small) part of the base-load of doing so. Not, therefore, legitimately to be entered in the "waste" column. But even if you don't entirely accept the wasted energy totals, more efficient supplies should appeal simply on grounds of engineering elegance, if nothing else.

The conversation with Mark Adams reminded me of a slightly different – but related – question he raised recently in a blog entry; Will the Internet of Things deliver power savings or will it be a massive power drain? On one side of this equation, many of the problems that the IoT aspires to solve are related to doing things more efficiently. There is the whole smart-grid domain, to take just one example: although much of that is concerned with limiting peak load rather the trimming absolute power levels. Monitoring the environment, shutting down what's not needed at any given instant: all very worthy.

But will there be an overall saving when you take into account the countervailing factor: there is going to be a lot of connected devices. Not all of them can be energy-harvesting, power-sipping motes or nodes, with minuscule duty cycles; big numbers are going to be network-connected, always-on and line-powered. Not to mention the build-up of infrastructure ("cloud", if you like) resources to service all the projected data-centric gadgets.

Mark Adams' commentary linked to, and reminded me of, a report issued in 2014 by the International Energy Agency (IEA), entitled Network Standby.

Its authors point to the proliferation of network-connected devices that (they say) maintain full network connectivity (or nearly so) when their top-level functionality is not being used and when they are notionally "in standby". Set-top boxes, games consoles, broadband modems and (as the IoT phenomenon develops) assorted gateways being cases in point. Some of those, the IEA report suggests, may run at as much as 80% of "on" levels when nominally in "standby". The report makes a plea for more sophisticated designs; *"Implementing best available technologies could reduce the energy demand of network-enabled devices by up to 65%. In the absence of strong market drivers to optimise the energy performance of these devices, policy intervention is needed."* More legislation, in other words.

You can, as I've said here before, make your own selection of number-of-billions of connected device that await us in our near future, from the many authoritative (or otherwise) forecasts that are out there. Whether you believe that the whole thing is overstated; or that we have only imagined a fraction of it: the idea that it will be net-energy-reductive looks very unlikely.

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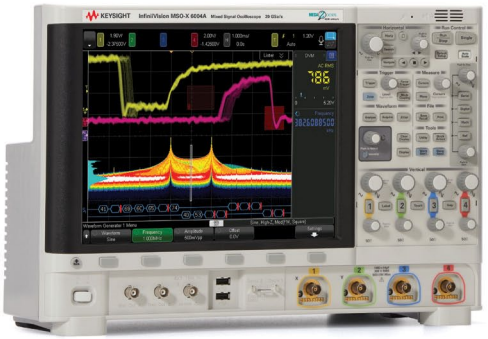

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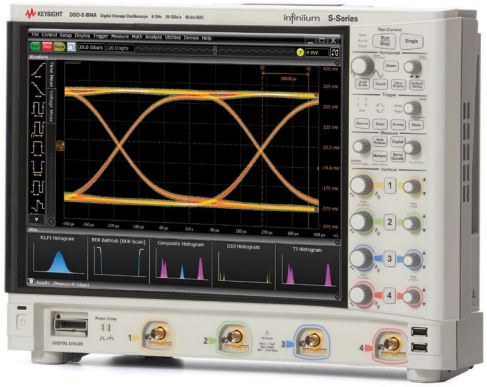

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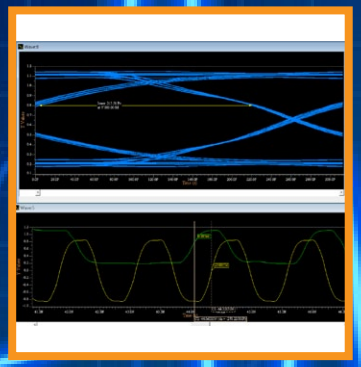

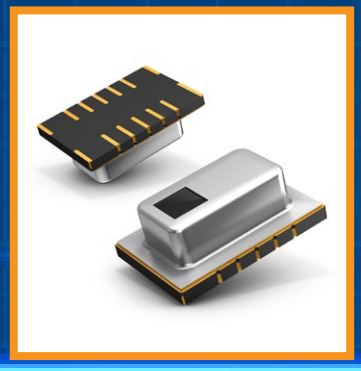

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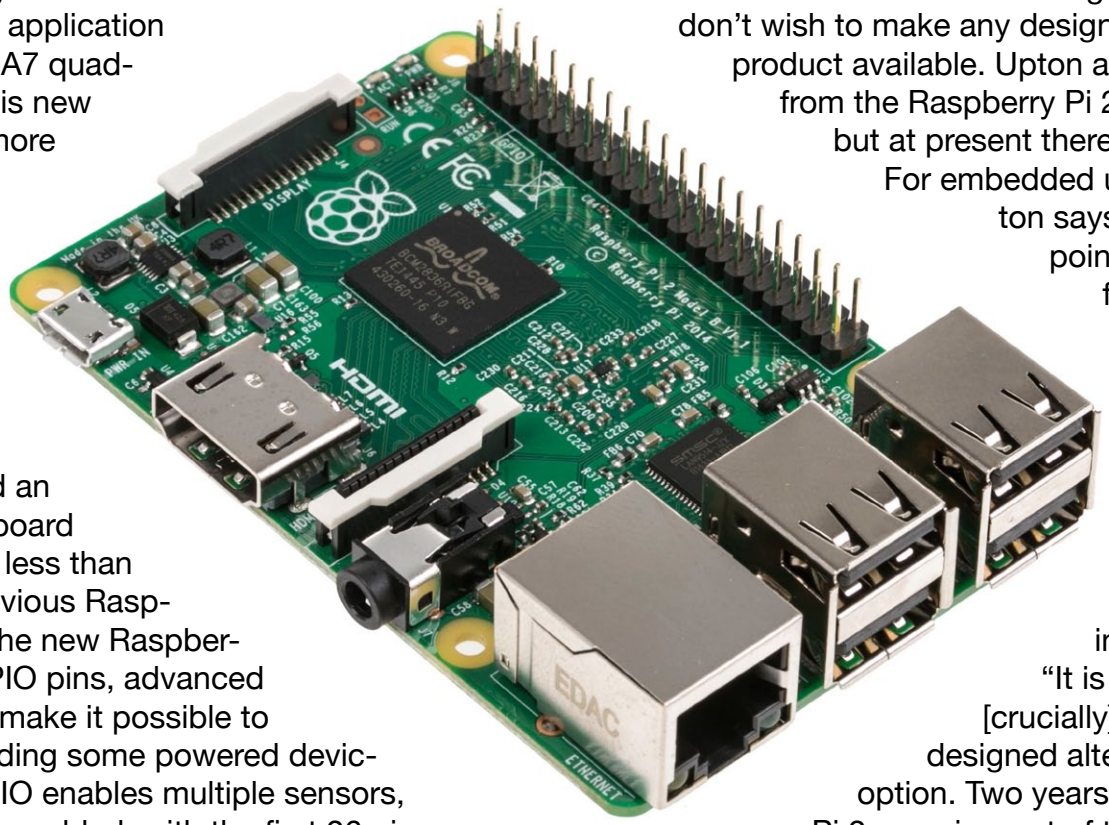
Raspberry Pi 2, model B; 6x processing power, 2x memory

The Raspberry Pi 2 Model B has four, faster processor cores and a doubling in memory capacity to 1 GB. The board incorporates the Broadcom BCM2836 application processor, containing an ARM Cortex-A7 quad-core CPU running at 800/900 MHz. This new processor makes the Raspberry Pi 2 more than six times more powerful than the first generation Raspberry Pi Model B+. The board layout, multimedia subsystem and peripherals remain fully compatible with the Raspberry Pi Model B+, including the use of the extensive 40-pin GPIO (General Purpose Input Output) connector, four USB ports and an efficient switching power supply. The board now hosts 1 GB of RAM, and boots in less than half the time of its predecessor. All previous Raspberry Pi projects are compatible with the new Raspberry Pi 2 Model B, and the expanded GPIO pins, advanced power management and connectivity, make it possible to connect up to four USB devices, including some powered devices such as hard drives. The 40-pin GPIO enables multiple sensors, connectors and expansion boards to be added, with the first 26 pins identical to the Model A and B boards, for full backward compatibility. Introducing the second-generation Raspberry Pi, founder Eben Upton offers some insights into the varied applications where he sees the Pi being used, in addition to its well-publicised role in education. Upton acknowledges that the first-generation Pi, while it could be used "as a PC", was at the limits of its performance in that role. Raspberry Pi 2, he says, marks, "a transition to a new world." In addition to the less demanding task it has been applied to – such as the education aspect – the new version will readily handle being deployed "just as a PC."



Embedded users who have designed in the existing model B+ and don't wish to make any design changes will continue to have that product available. Upton adds that a compute module derived from the Raspberry Pi 2 is an anticipated project/product, but at present there is no projected date for its release.

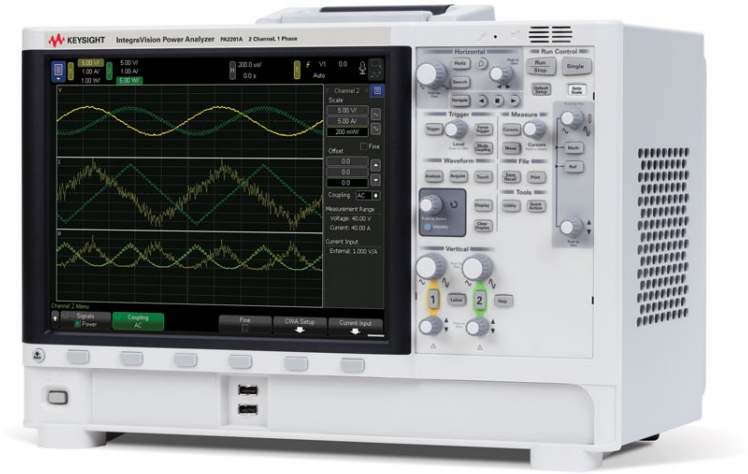
For embedded use of the compute module, Upton says that his objective is to get to the point – both from the supply side, and from users perceptions – where, "it makes no sense not to use it at any volume under 50,000 units." Upton adds that Raspberry Pi has seen varied deployment in embedded functions, often in control and supervisory roles in larger items of equipment. He sees the Pi being valued in that context because, "It is cheaper, has higher reliability, and [crucially] better stability," than a custom-designed alternative or any other off-the-shelf option. Two years of engineering has gone into the Pi 2; a major part of this has been in cost-reduction, so that the board can be manufactured and delivered for the same price as the first-generation issue; but also into ensuring stability and reliability.

Click right and also here.

Complete article, here

AC power analysis and oscilloscope display, in a single instrument

Keysight Technologies has introduced a power analyser with touch-operated oscilloscope waveform display functions; engineers will no longer need two separate instruments to characterise power waveforms. There will be two basic versions, for single-phase and 3-phase power analysis. Combining accurate power measurements and touch-driven oscilloscope waveform viewing capability in a single instrument, the IntegraVision power analyser is intended for engineers who are designing and testing electronic power conversion systems to access dynamic views of current, voltage and power, in projects such as power inverters or converters, universal power supplies, battery systems, vehicle and aircraft power systems, lighting systems/electronic ballasts and appliances.



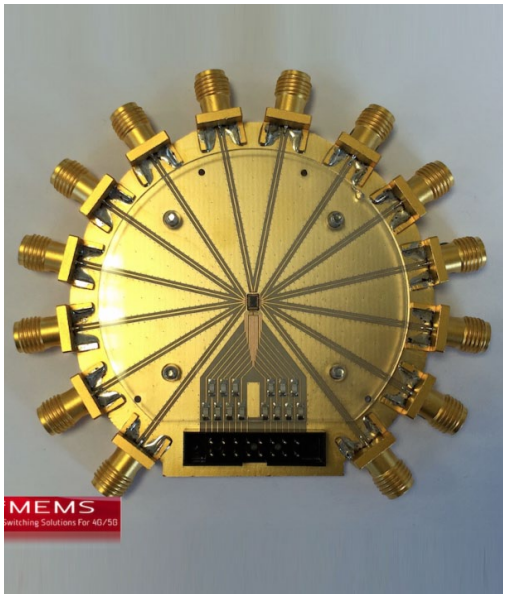
The IntegraVision power analyser has isolated inputs rated up to 1,000 Vrms (Cat II). The instruments offer external sensor inputs and 2A(RMS) and 50 A(RMS) direct current inputs, standard on all channels. The external sensor input supports current probes and transducers up to 10V full scale. Eliminating a separate oscilloscope in the measurement setup decreases test complexity and reduces configuration time, Keysight says; its IntegraVision power analysers are designed to quickly and interactively measure AC and DC power consumption, power conversion efficiency, operational response to stimulus, and common AC power parameters such as frequency, phase and harmonics – all with 0.05% basic accuracy and 16-bit resolution. The power analyser enables engineers to characterise power consumption under highly dynamic conditions with 5 Msamples/sec digitising rate and 2 MHz bandwidth.

Complete article, here

12-way RF MEMS ohmic switch targets LTE-A handsets

A SP12T switch made using DelfMEMS' FreeFlex MEMS technology will, the company says, deliver the performance needed for next generation smartphone handsets. The developer of RF MEMS switching solutions will demonstrate what it believes to be the first twelve throw, RF MEMS ohmic contact switch at Mobile World Congress (MWC) 2015.
Cybele Rolland, DelfMEMS CEO, explains, "Until now, companies have tended towards the capacitive switch solution route. We chose the harder route of contact or Ohmic switching because of the superior performance and have succeeded in creating the world's first, fully functional version..."
The potential benefits of DelfMEMS RF-MEMS switching solution are being able to deliver the performance required for the next generation of handsets, LTE-A and beyond, with ultra-low in-

sertion loss, outstanding isolation and superior linearity to enable full uplink carrier aggregation.
The early samples of the SP12T switch, which will be shown at MWC, have performance levels that are comparable to the current



market leading solutions but for production devices the company expects performance levels will be significantly higher, enabling the full potential of LTE-A, and beyond, data rates for both upload and download to finally be achieved.

Complete article, here

Blue-light optical encoder ICs boost resolution and performance

iC-Haus has developed sensor chips for optical position encoders with photodiodes optimised for blue wavelengths. The shorter wavelength and penetration of blue-light photons can improve the resolution, signal amplitude, harmonic distortion, and jitter performance of incremental and absolute encoders, the company says. Blue light causes less diffraction at the same slot width compared to higher wavelengths, thus resulting in sharper imaging. Modern semiconductor processes provide small, shallow structures which can take advantage of the shorter penetration of blue light to improve efficiency. Smaller structures allow an interlaced photodiode layout which produces sine and cosine encoder signals with lower offset. In addition, a high fillfactor for the photosensitive areas is achieved by an equivalent geometrical transformation.

Long term temperature-stable blue LEDs are available, iC-Haus continues, which outperform the IR and red LEDs used in encoders so far, because they offer higher light yield and efficiency at lower cost. Optical position sensors benefit as a result of the technological progress of both LED and CMOS technology. iC-Haus has optimised its incremental scanners in its high resolution iCPT H Series for blue light, undet the platform name Encoder blue. The encoder chips combine optimised scanning and signal interpolation in the smallest available space: a flat 5 x 5 mm optoQFN package with a plane window. Due to the phased-array structure of the optochips, a minimal scanning area of only 1.9 x 3.1 mm is sufficient to generate 10,000 pulses per revolution using a code disc of 26mm diameter.

Complete article, here

Snapshot hyperspectral image sensors use mosaic filters

Belgian research centre imec has disclosed a new set of snapshot hyperspectral CMOS image sensors featuring spectral filter structures in a mosaic layout, processed per-pixel on 4x4 and 5x5 'Bayer-like' arrays. These hyperspectral filter structures are processed at wafer-level on commercially available CMOS image sensor wafers, enabling extremely compact, low cost and mass-producible hyperspectral (multi-wavelength, beyond the visible) imaging solutions. This paves the way, imec says, to applications ranging from machine vision, medical imaging, precision agriculture to higher volume industries such as security, automotive and consumer electronic devices.

Andy Lambrechts, program manager at imec, comments, "The new mosaic architecture, and extended spectral range, brings unique advantages compared to our previously announced hyperspectral linescan sensors for applications in which scanning would not be practical. It enables spectral imaging in a truly compact, tiny form-factor, that can even be scaled to handheld devices. From the technology standpoint, we have now successfully demonstrated linescan and tiled sensors, in which spectral filters cover many pixels, to mosaic sensors, in which filters vary from pixel to pixel. At the same time, the spectral range is extended and now covers down to 470 nm."

The newly developed mosaic sensors feature one spectral filter per pixel, arranged in mosaics of 4x4 (16 spectral bands) or 5x5 (25 spectral bands) deposited onto a full array of 2 Million pixels 5.5 µm size CMOSIS CMV2000 sensor.

Complete article, here

ARM MCU built in sub-threshold technology for 10-fold power reduction

Ambiq Micro says its Apollo microcontrollers redefine 'low power' with up to 10x reduction in energy consumption: the ARM Cortex-M4F microcontrollers are based on subthreshold voltage technology.

Ambiq Micro, based in Austin, Texas, says it has resolved the issues surrounding placing logic built with sub-threshold technology into volume production in a standard CMOS process. Its first announced products are the Apollo family of four 32-bit ARM Cortex-M4F microcontrollers (MCUs). In real-world applications, their energy consumption is typically 5 to 10 times lower than that of MCUs of comparable performance, resulting in far longer battery life in wearable electronics and other battery-powered applications. The reduction in energy consumption is achieved using Ambiq's patented Subthreshold Power Optimized Technology (SPOT) platform.

In sub-threshold logic, individual transistors are never turned completely on; effectively, logic levels are propagated as leakage-current or leakage-current-plus-a-bit. Dissipation is greatly reduced but the generation and detection of logic levels, and execution of logic functions, has to be stable in the face of process variations, noise, temperature drift and a range of other variables. Previous successful attempts to use sub-threshold logic (watch ICs, for example) have most often been built in in-house, dedicated fabs where process variables have been constantly tuned and refined. Ambiq's claim is that it has designed structures that can maintain correct operation when implemented in a stock foundry CMOS process.

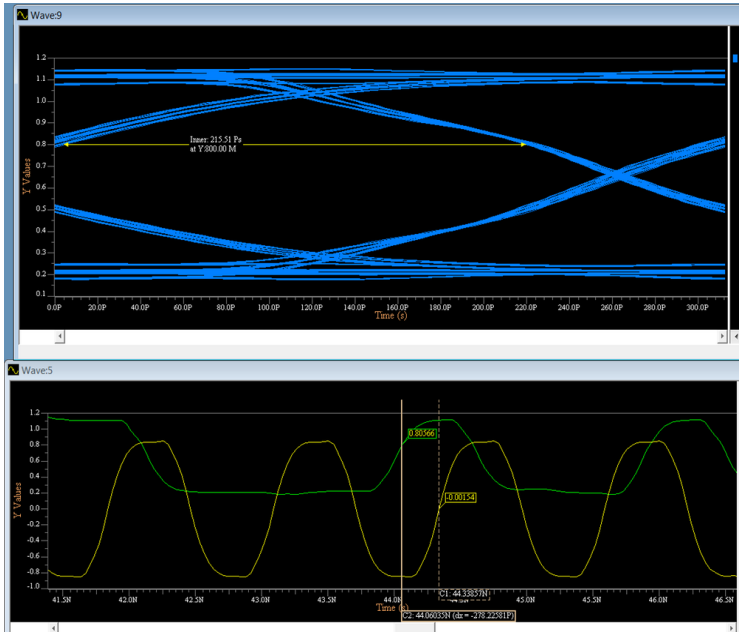
"We do have to do work at the RTL level," says a company spokesman, "But the IP of the ARM MCU is untouched – this is a standard ARM core, with the floating point unit." All of the benefits to power flow from the sub-

threshold implementation. Apollo MCUs optimise both active and sleep mode power (the two factors are mutually contradictory in a conventional process, the company explains). They consume 30 µA/MHz when executing instructions from flash and feature average sleep mode currents as low as 100 nA. Apollo MCUs operate at up to 24 MHz. They are available with up to 512 kB of flash and 64 kB of RAM to accommodate radio and sensor overhead in addition to application code. Communication with sensors, radios, other peripherals and an optional host processor is implemented via I²C/SPI ports and a UART. On-chip resources include a 10 bit, 13-channel, 1 Msample/sec ADC and a temperature sensor with ±2°C accuracy. Two compact packaging options are available – a 64-pin, 4.5 x 4.5 mm BGA package with 50 GPIO and a further size-optimised 2.4 x 2.77mm, 42-pin CSP with 27 GPIO.

Complete article, here

"Virtual-lab" environment provides exemplars of advanced PCB design flows

Mentor Graphics has secured the participation of a number of industry players who make leading-edge – especially, high-speed signalling – devices, to demonstrate the capabilities of its HyperLynx design environment for advanced and high-speed PCBs. The HyperLynx Alliance has been formed by Mentor Graphics and industry partners to provides free access to virtual reference designs plus tools, design data and identified best-practice methodologies for difficult SerDes and DDR design and verification challenges; companies involved from the outset are Altera, PMC-Sierra, Samtec, Inc. and eASIC.



Noting that new high-speed protocols are increasingly difficult to design and verify at multi-gigabit speeds, the Alliance cloud platform provides access to targeted vendor reference designs, tools and models, allowing engineers to evaluate and tradeoff device parameters using recommended verification methodologies and sample channel designs. Virtual labs [modules or sessions] include the complete HyperLynx design environment, partner IBIS-AMI electrical models, a reference design for test cases, and a step-by-step instruction guide. Each HyperLynx virtual lab can be completed in a few hours and is available as a future resource for users during real design and implementation stages. The alliance uses the HyperLynx tool suite for high-speed design and verification, deployed on cloud-based virtual labs to accelerate time to productivity. The virtual lab series uses partner models and reference designs with the tool suite to demonstrate ideal design methodologies to address difficult high-speed printed circuit board (PCB) SerDes and DDR design challenges. The virtual labs reduce engineering time and costs associated with evaluation design tool requests and design case setup which could take days or weeks. The labs walk through a recommended design process, helping engineers formulate their own methodologies and enabling them to evaluate trade-offs to improve overall system performance.

Complete article, here

Infineon, Hella make radar sensor more affordable

by Christoph Hammerschmidt

Infineon and German tier one automotive equipment maker Hella KG now have jointly developed RF components for radar sensors that enable manufacturers to lower prices and power consumption. Hella already produces a 24-GHz radar sensor system for blind spots. This continuously updated radar scan detects moving objects even in poor weather and independent of the direction and speed of their motion. Optimised antenna concepts facilitate an even higher measuring accuracy. Infineon's Microwave Monolithic Integrated Circuit (MMIC) using the BGT24Axx chip family, helps to increase the detection efficiency of the driver assistance system.

It improves the signal-to-noise ratio (SNR), ensuring higher precision in the detection of objects in the blind spot. The MMICs integrate all RF components such as oscillators, amplifiers and reception branches with low-noise amplifiers and I/Q mixers on a single chip. Hella's radar system can be smaller, more affordable and it consumes less power. The 24GHz chip family enables a custom-fit configuration of the hardware, depending on the system environment and application field.

Complete article, here

New magnetic materials seek memory, wireless applications

A class of structures called hybrid multiferroics may yield improved data storage and new wireless applications. To exploit and control magnetism, technology often relies on electromagnets, which limit hardware configurations due to their size and energy consumption. As an alternative, researchers are beginning to develop hybrid nanomaterials that are responsive to both electric and magnetic fields. These materials can save energy and space, and may open up new applications. Power savings are one incentive, but another factor is the multi-functionality they could offer, possibly leading to new forms of information storage.

"Some materials exhibit spontaneous electric or magnetic order. These materials are called ferroelectric and ferromagnetic, respectively," explains Professor Sebastiaan van Dijken, leader of the Nanomagnetism and Spintronics Group at Aalto University, Espoo, Finland. "However, among these two ferroic materials there is little overlap." Prof. Van Dijken's group received a €1.5million European Union grant in 2012, to fund a five-year project. To further its investigations, the group has developed a microscopy technique that employs an ultra-fast camera, to enable the imaging of ferroelectric-ferromagnetic coupling effects in an applied electric field with nanosecond-precision. Study objectives include finding out if, and how, it is possible to manipulate the magnetic properties of materials by electrical means in nanoscale structures and in the time frame of nanoseconds. Professor van Dijken's team have been creating hybrid structures using one stable ferroelectric material and one stable ferromagnetic material. Built at the nanoscale, thin films of each material are linked together by strong coupling at their interfaces, enabling them to be used as a single entity.

Complete article, here

Valydate schematic design analysis and verification now on Altium

Altium and Valydate, writers of software for schematic, signal and power integrity analysis, have entered a partnership aimed at easing the time-consuming visual inspection and debugging process of electronic schematics, by integrating the design analysis and verification tool ValydateVERA into Altium Designer. The two companies say that the technology will aid in streamlining the design process and save designers hours in visually inspecting of schematics for errors.

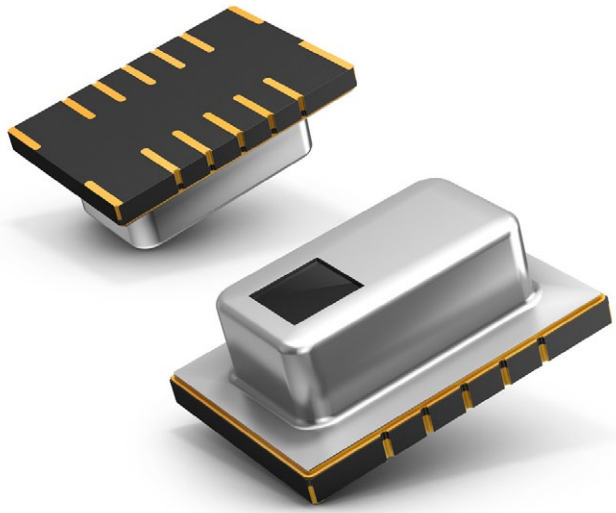
The rising complexity of modern electronics design has ushered in a multiplying set of rules and verifications that must be manually checked for schematic design errors, regardless of which design software is used. Requiring manual validation has a dramatic impact on schedules. ValydateVERA claims to effectively streamline this process. With VERA's integration in Altium Designer, designers can now automatically inspect their schematics against a predefined checklist that takes advantage of an intelligent component library that automatically checks for thousands of error violations in schematic designs.

"We've seen a steadily increasing number of customers working with complex designs who had no choice but to manually check their schematics for thousands of potential errors which adds up to countless wasted hours," said Jason Hingston, CTO at Altium.

Complete article, here

Thermopile array sensor identifies movement, direction and multiple objects

Panasonic Automotive & Industrial Systems has introduced what it believes to be the first surface mount thermopile array sensor. Grid-EYE features 64 thermopile elements in an 8x8 grid format that detect absolute temperatures by infrared radiation. Grid-EYE is able to measure actual temperature and temperature gradients, providing thermal images. It is possible to detect multiple persons, identify positions and direction of movement, almost independent of ambient light conditions without disturbing privacy as with conventional cameras.



Cost-effective and compact solutions for contactless temperature measurement across the entire specified area can configured with very accurate results. A built-in silicon lens provides a viewing angle of 60°. Measurement values can be read out via I²C interface in 1 or 10 frames per second. An interrupt signal output delivers a quick response to time-critical events or additional energy saving capabilities in stand-by mode, offering a high degree of flexibility.

Measuring 11.6 x 4.3 x 8.0mm, Grid-EYE arrays have an operating voltage of 3.3V or 5V and a typical current consumption of 4.5 mA (normal mode); 0.8 mA (stand-by mode); and 0.2 mA (sleep mode). Object temperature range is 0 to 80°C for the high gain amplification version and -20 to 100°C with low gain. Overall Temperature accuracy is ±2.5°C with an NETD (Noise Equivalent Temperature Difference) of ±0.5°C, depending on P/N.

Complete article, here

PC-based scopes use USB 3.0, offer 512 Msample memory depth

PicoScope 3000D Series oscilloscopes have up to 200 MHz bandwidth, two or four analogue channels plus 16 digital channels on the mixed-signal (MSO) models, and deep memories from 64 to 512 mega-samples. The scopes offer a maximum real-time sampling rate of 1 Gsample/sec and feature a USB 3.0 interface; they also host a built-in arbitrary waveform generator (AWG). Deep memory enables long timebases with the fastest sampling rates; for example, at 1 Gsample/sec sampling rate you can capture a 500 msec waveform—that's half a billion samples, Pico points out—while hardware acceleration keeps the display updating smoothly.

The 512 Msample buffer memory can be segmented, enabling acquisition of up to 10 000 individual waveform segments of 50 000 samples, with less than 1 µsec rearm time between each segment. The oscilloscopes are multi-function, including a spectrum analyser and arbitrary waveform generator (AWG), and advanced functions as standard, such as serial bus decoding, mask limit testing, maths channels and filtering.

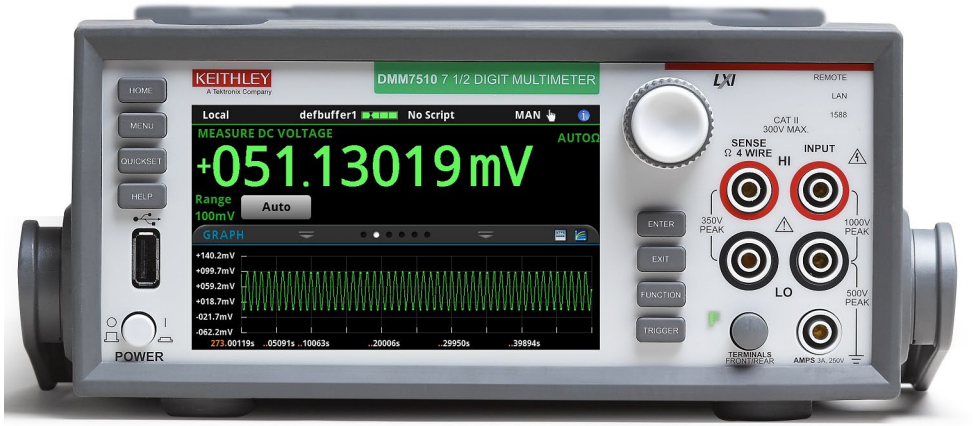
Advanced triggers include pulse width, interval, window, window pulse width, level dropout, window dropout, runt pulse, variable hysteresis, and logic. All triggering is digital, ensuring low jitter, high accuracy and single-LSB voltage resolution. MSO models combine these triggers with edge and pattern triggering on the digital inputs. Features include colour persistence display modes, automatic measurements with statistics, programmable alarms, and decoding of I²C, UART/RS232, SPI, CAN bus, LIN, FlexRay and I²S signals. Software updates include a fast persistence mode that gives updates of around 100 000 waveforms per second, while the math channels have been expanded to include configurable filters.

Complete article, here

7½-digit DMM has 1 MHz sampling, plus graphical display

Termed by Keithley the first "graphical sampling digital multimeter" the DMM7510 combines high accuracy, integrated data visualisation, and operation via a capacitive touch screen with an interface that is modelled on the "smartphone experience". The DMM integrates a high accuracy digital multimeter, a digitiser for waveform capture, and a capacitive touchscreen user interface. Keithley says that the design philosophy of the instrument is based on helping engineers to get an in-depth understanding of their devices under test, in a context where they need to capture small signals at higher accuracy and faster speeds than traditional DMMs can provide. The Model DMM7510 uses an 18-bit conversion, with a peak sampling rate of 1 Msample/sec. Basic accuracy is 14 ppm (parts-per-million). It can display a graphical representation

of the captured samples, but Keithley is careful to point out that this is not updated as is a scope display.
You operate the instrument with a graphical touchscreen which responds to a range of gestures (swipe, etc.) that are borrowed from smartphone and tablet computer practice (or by means of conventional rotary-knob control), and there is internal processing to carry out analysis of the captured data points.
Resolution level is selectable from 3½ to 7½ digits; the unit provides DC accuracies "typically only found in metrology-grade instrumentation—but at about half the price of those solutions" the company asserts. The 14ppm basic 1-year accuracy applies to DC voltage measurements. Expanded measurement ranges (100 mV, 1Ω, and 10 µA) enhance low level accuracy. On the 10 µA range, resolution is therefore 1 pA: at the other end of the scale, the 7510 has a 10A current range, without use of external shunts.



Complete article, here

ARM adds safety support to Cortex-R5 IP for automotive, medical and industrial markets

ARM has created a comprehensive safety document set for the ARM Cortex-R5 processor to assist its adoption in safety-critical applications. The Cortex-R5 is the first in a range of ARM processors to come with a safety document set that semiconductor companies can use to demonstrate compliance with new functional safety standards.
ARM notes the importance of functional safety in markets that include automotive, medical and industrial applications, and says, "The Cortex-R5 processor has a rich set of fault detection and control features and the addition of generic safety documentation means developers can now use it across the broadest range of safety applications." Part of the context, ARM notes, is that the applicable standards have evolved and recognise the role of IP, enabling ARM address the issue of functional safety directly.
The work it has done, ARM says, is at several levels; it offers support for safety-related operations and functions (dual-core lock-step operation, for example) but also provides documentation that covers not only the IP itself but the methodologies of its design. A significant proportion of the preparation for this release has, the company says, been related to process; the design process must stand up to scrutiny regarding its approach to design-for-safety and how that has been applied at all stages.
This complements the fact that the company has included fault detection and control features in its IP for many years. The offering is "standards agnostic" that is re-usable across different market sectors; it supports a range of safety levels (for example, the tiered SIL structure in automotive/industrial contexts) and is configurable, and modular. ARM has already worked with its licensees in this area, citing Texas Instruments, which offers a safety-critical-systems application and documentation package with its Hercules MCUs.

Complete article, here

GPU COMPUTE AND OPENCL: AN INTRODUCTION – PART 2

By Nicu Penisoara, Freescale Semiconductor

This article provides to the reader unfamiliar with the subject an introduction to the GPU evolution, current architecture, and suitability for compute intensive applications. OpenCL was introduced in this context (in the first part of the article), and in this second part a sample application is presented, together with indications on setting up the development environment, building and running the application on a Freescale i.MX6-based platform.

Editor's note; Part 1 of this article is here; the pdf download accessed by clicking the link below contains Part 1 and Part 2.

Overall setup and OpenCL application overview

As the reader remembers from the first part of the article, any OpenCL application has two components: one that runs on the Host (for system management, as well as control code) and a second one that runs on the Compute Device(s), typically doing the "heavy lifting" in terms of data processing. While in some systems (for example, a typical PC equipped with a graphics card), these two entities are physically separate devices, in a vast array of modern Application Processors we have available an integrated GPU, capable of running OpenCL applications.

For our demo application we will use the same i.MX6 Quad SoC that we have referred to in the first part of the article to exemplify the structure of a modern GPU from an OpenCL perspective. The Host is represented by the cluster of four ARM Cortex A9 CPUs, while the Compute Device is represented by the GC2000 GPU. As a system to run our demo application we have chosen the i.MX6 Sabre SDB, one of the reference hardware platforms for this SoC – pictured in Figure 1.

While potentially a little ambitious for a "Hello World" type application, we will put the screen of the SABRE platform to use in our applica-

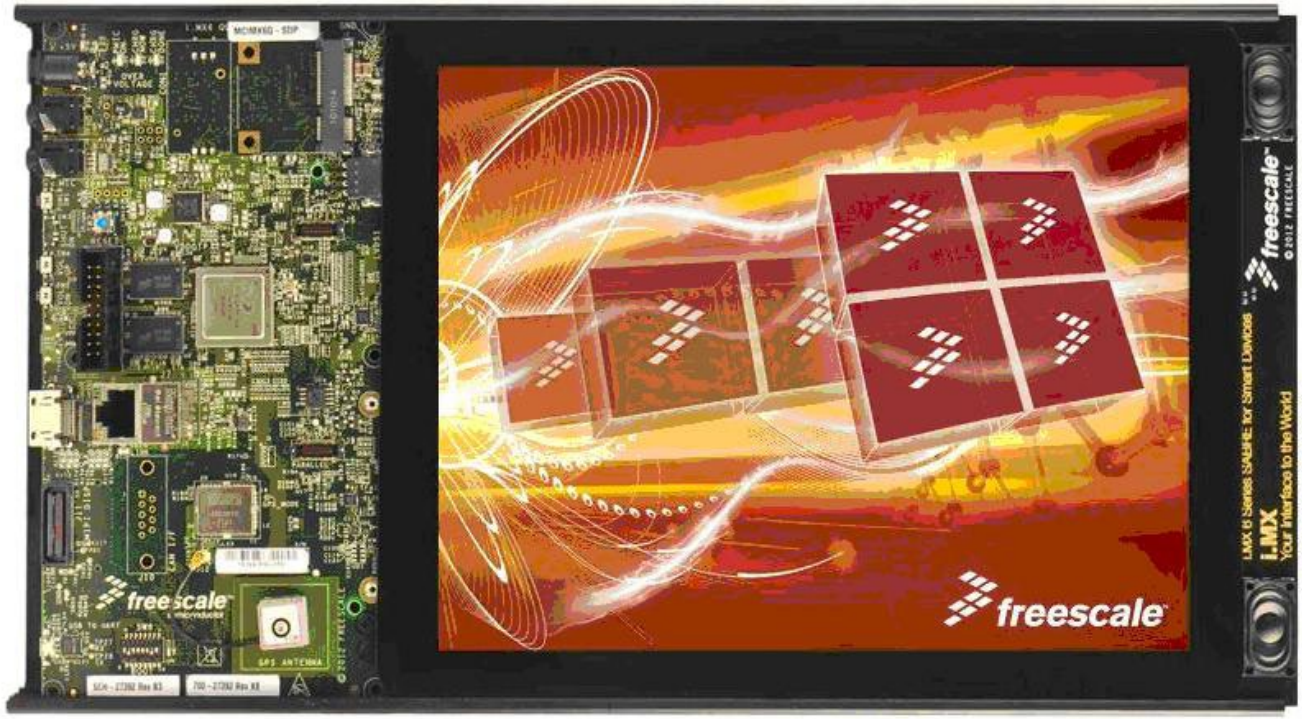


Figure 1. *SABRE platform for Smart Devices based on I.MX6*

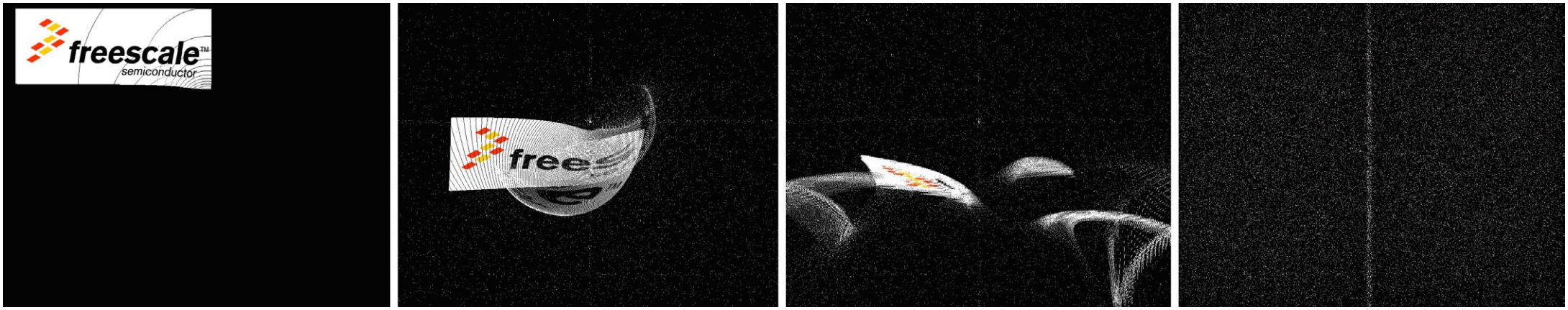


Figure 2. *Demo application output on the LCD screen*

tion, as we will present an application that represents the movement of a particle system under the action of predefined forces in a closed system, with the initial set of particles given by a bitmap. Figure 2 above captures the screen output at different stages in the application execution (or particle system lifetime).

Hoping that we have generated enough interest such that reader will venture into replicating and tinkering with the application, we will look in the next sections at the system setup, Host as well as Compute device applications.

System setup

As a development environment for the Host we will use C under Linux. In order to build and boot a Linux system on our SABRE board, we will use the latest Freescale Linux BSP release, available on www.freescale.com , in the "Software and Tools/Software development tools" section for the i.MX6 application processor - at the time of the writing, the latest Linux BSP release is L3_10_53_1.1.0.

After downloading the BSP, the steps needed to build the Linux image and boot it on the target system are presented in the "Freescale Yocto Project User's Guide" document. As for the OpenCL demo application we will use frame buffer, the recommended image to build and deploy is "fsl-image-gui" – this image has all the needed libraries required by our application.

If you want to replicate this demo on other i.MX6 based system, it is important to note that the requirements for the Linux image booted on the target are to have the gpu-viv-bin-mx6q package selected, as well as frame buffer support.

Click below for the complete article download.

BRING SECURITY INTO DEVELOPMENT AND VERIFICATION

By Mike Bartley & Declan O'Riordan, TVS

Autonomous systems require particular attention to security and trustworthiness before deployment.

Increases in processing performance and the growing pervasiveness of communications are making it possible to create a new generation of autonomous systems, including self-guided drones and automated road vehicles as well as sophisticated industrial control systems. Many of these systems will be fed data by an array of distributed sensors, giving them much better information about their environment, allowing them to make intelligent decisions.

But the number of inputs and their connectivity to other systems on the internet provides these autonomous systems with a large attack surface, offering many possible opportunities for attackers to disrupt their operation and either take control or cause them to crash. As a result, designers of these autonomous systems need not only design for safety but take security into account in the design to ensure that the system does not become unsafe if attacked.

Numerous reports of attacks, which have increasingly focused on embedded systems such as those used to control point-of-sale (POS) systems, show how limited the industry's attention to secure design has been. Many of these penetrations by hackers have been through mistakes made in system design and implementation.

According to the IEEE Centre for Secure Design, design flaws account for 50% of software security issues, and these flaws take many forms. The Massachusetts Institute of Technology Research (MITRE) has identified 700 different kinds of software security weakness. Any given system may only have a fraction of those weaknesses but as attackers will target the weakest part of the system, even a few flaws can lead to a successful penetration.

There is a need to define a development strategy that takes into account all aspects of a design that can lead to unsafe and unwanted behaviour – whether caused by intentional harm or noise in the system. The requirement is for systems that remain trustworthy in the face of external influences. To address the issue of unreliable and potentially unsafe software and systems, the Trustworthy Software Initiative

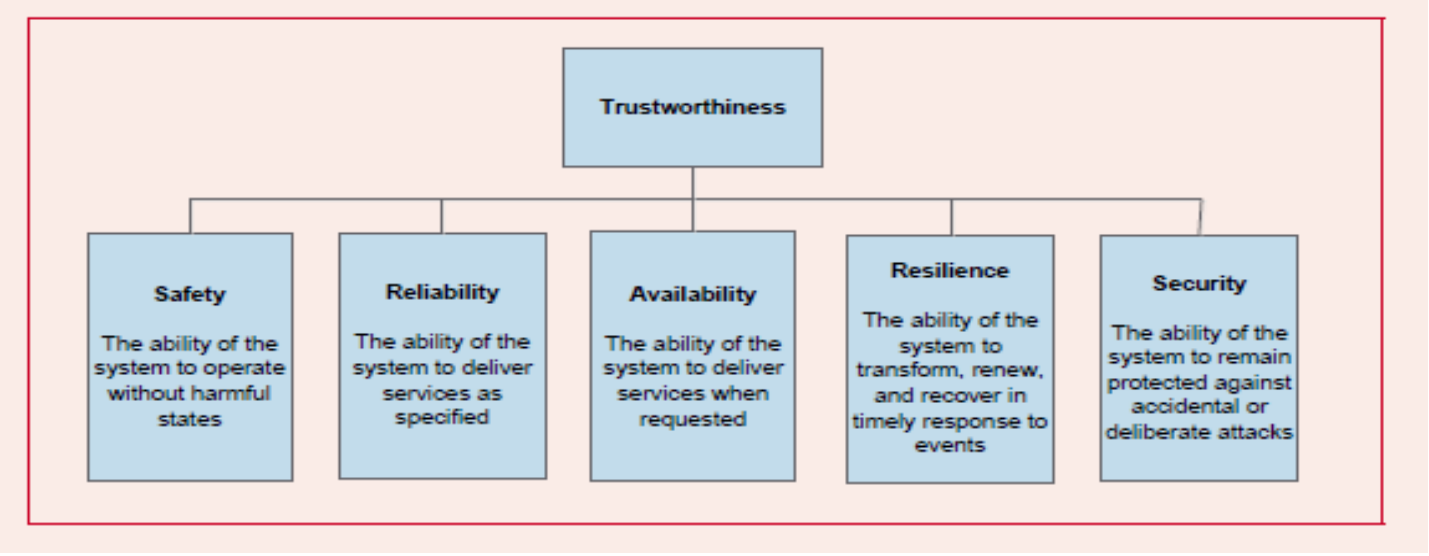


Figure 1. *The PAS 754:2014 standard identifies five aspects of software trustworthiness.*

backed the British Standards Institute's PAS 754:2014 standard, which identifies five aspects of software trustworthiness: safety, reliability, availability, resilience and security (Figure 1).

An important principle of building secure and trustworthy software is that security cannot be "tested in": security needs to be built in. Test is part of the overall development cycle that ensures that security and trustworthiness concerns have been addressed properly.

The BSI document describes a widely applicable approach to achieving software trustworthiness rather than mandating any specific practices or procedures. The standard calls for an appropriate set of governance and management measures to be set up before producing or using any software which has a trustworthiness requirement. PAS 754 is designed to support the building of systems that can protect themselves against both accidental and deliberate attacks.

Under the regime, design teams need to perform risk assessments that consider the set of assets to be protected, the nature of the adversaries that may be faced and the way in which the software may be susceptible to such challenges. From a security perspective, this includes threat assessments to determine how attacks may be made either directly or indirectly. For example, in an IoT system, an attacker will focus on the weakest nodes. These could be subverted into performing denial of service attacks on other nodes in the system, causing them to fail or to bring the whole system down even though they are not vulnerable to a direct penetration attack.

To manage risks and threats, appropriate personnel, physical, procedural and technical controls need to be deployed. Finally, PAS 754 demands a regime be set up to ensure that creators and users of software confirm that governance, risk and control decisions have been implemented.

In the continuation of this article, the authors develop the idea of a structured methodology for software development that moves consideration of security earlier in the process. Click below.

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HIGH DYNAMIC RANGE IF RECEIVER MICROWAVE MODEM DESIGN

By Paul Hendriks, Analog Devices

Microwave point to point links are an integral part of a cellular mobile network providing backhaul capability between cell sites (BTS/NodeBs) and the radio controllers (BSC/RNCs) in over 50% of global deployments where fibre links are not cost effective to deploy.

The recent explosion in mobile network traffic driven by the market shift to smartphones (i.e streaming video) has intensified data demands and put pressure on the existing existing microwave backhaul equipment capacity. In order to scale the data throughput of the backhaul network to the needs of LTE and LTE-Advanced, the next generation microwave links will need to :

- Move to increasingly higher order digital modulation from today's QAM256 to as high as QAM4096 in the future, thus providing a 50% increase in capacity within a fixed channel assignment.
- Support channel assignments from 56 MHz today to 112 MHz in the traditional 6-42 GHz band. Every doubling of channel bandwidth provides a proportional increase in the data throughput rate capability if the Carrier-to-Noise Ration (CNR) remains constant.
- Employ techniques such as polarisation diversity, channel aggregation and NxN Line-of-Sight MIMO.

As is typically the case in communication system design, this increase in throughput capability does come at a price. To support combinations of higher QAM levels and channel bandwidth, the microwave link must have more dynamic range capability to support the required minimum EVM performance performance since receiver sensitivity is reduced by 3 dB for every doubling in QAM size or bandwidth. Since the microwave equipment must remain flexible, additional consideration is required to support all possible operating scenarios while still simplifying the Rx filtering and AGC requirements for improved performance and cost reduction.

An additional industry trend is the emergence of full outdoor units (ODU) in which the full radio modem and transceiver are combined with the switching/multiplexing units and traffic interface in a self-contained box mounted on a tower or equivalent structure. This trend is driven by CAPEX/OPEX at new sites and space constraints at existing sites. Traditional "split" indoor(IDU)/outdoor(ODU) systems systems host the µW/RF section in the ODU with a coaxial cable connecting to the rest of the system housed in a equipment shelter (IDU). The coaxial cable can be up to 300 metres in length and carries bi-directional traffic with a diplexer being used to separate the Rx IF signal centred at 140 MHz from the Tx IF signal being centred in the 340-400 MHz range.

While this is a noteworthy trend, the majority of µW equipment shipped today and in the foreseeable future is the legacy split IDU/ODU system. It would be beneficial to use one back-end modem transceiver architecture for design re-use purposes that supports both the legacy system and the next-generation ODU platforms. Recent advances in both high speed DAC and ADC technology operating at clock rates well above 1.5 Gsamples/sec are now making it possible to synthesise and digitise QAM signals at high IFs with exceptional accuracy to support 4096 QAM (and beyond). Besides eliminating the need for any quadrature error correction required for traditional analogue IQ implementations, the high dynamic range along with high oversampling ratio allows the majority of the filtering to be performed in the digital domain thus reducing the amount analogue filtering and digital equalisation required to compensate for them. For the Tx signal path, high-speed DACs such as the AD9142 and AD9136 are already beginning to replace the traditional dual DAC and IQ

modulator implementations to synthesise the wideband QAM signals with exceptional EVM (error vector magnitude) performance without the need for Tx calibration. For the Rx signal path, the availability of 1.5+ Gsamples/sec ADCs well suited for these applications has lagged until the recent release of the AD6676.

The AD6676 is the industry's first wideband IF Rx subsystem (Figure 1) based on a bandpass sigma-delta ADC supporting IF signal bandwidths up to 160 MHz while operating with an internal clock rate of up to 3.2 GHz. It is the high oversampling capability of the Σ-Δ ADC that greatly simplifies the IF analogue filtering requirements required in lower sampling ADCs to suppress adjacent channels (and interference/blockers) that would otherwise "alias" back onto the IF signal thus reducing the receiver's sensitivity performance. Also, it is the ADC's high dynamic range with an NSD (noise spectral density) floor of -160 dBFS/Hz (for narrowband QAM channels) that reduces the diplexer Tx-to-Rx isolation requirement or analogue AGC range that compensates for fading.

This article continues by illustrating how this new generation of ADCs can simplify traditional transceiver design, and goes on to discuss how it enables the use of higher-order QAM without adding filter complexity. Click right, for the complete article download.

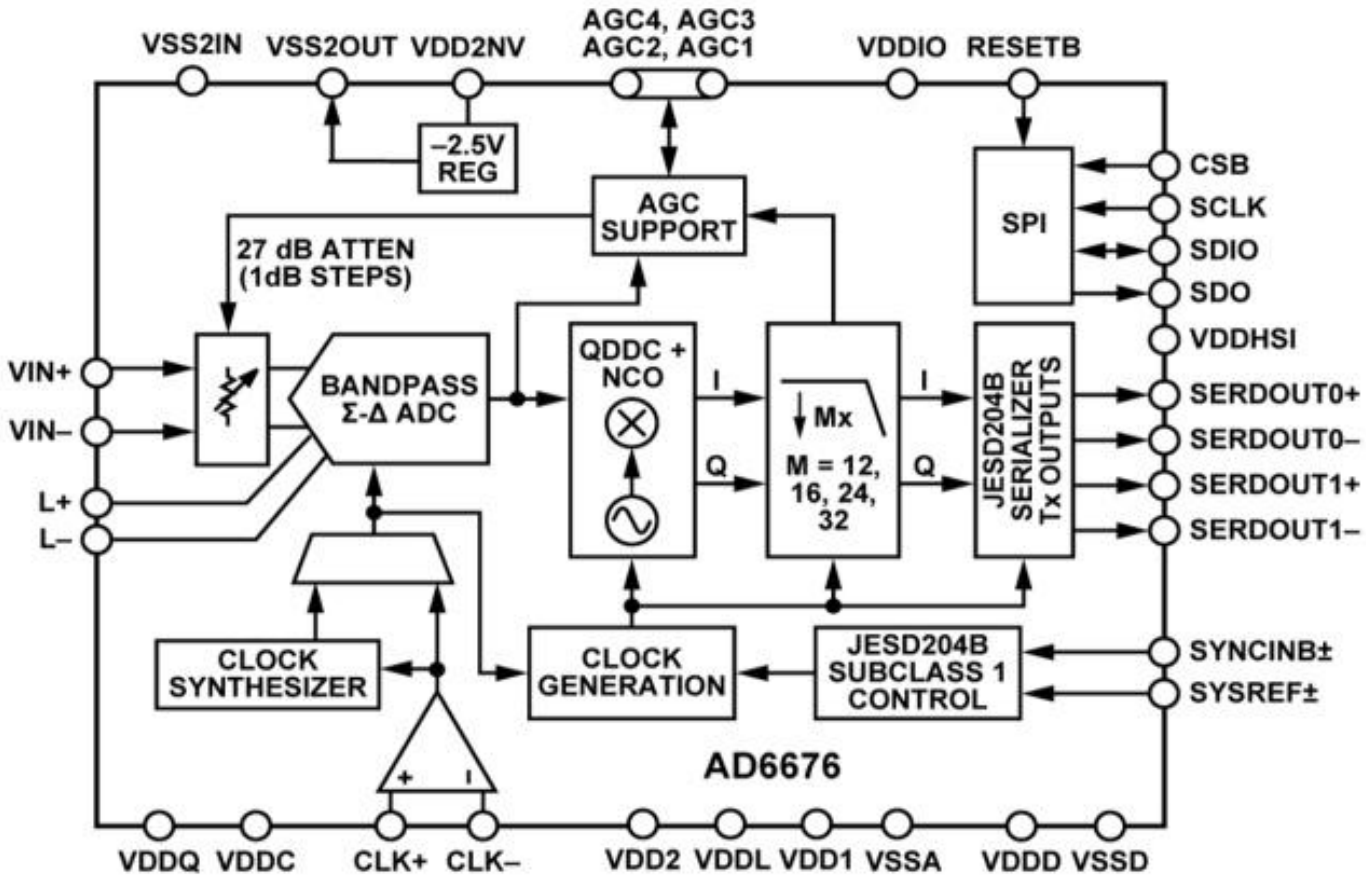

Figure 1. *Block diagram of the AD6676 IF Rx Subsystem*

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CHOOSING THE RIGHT WIRELESS MESH NETWORK PROTOCOL FOR THE INDUSTRIAL INTERNET OF THINGS

By Ross Yu, Dust Networks

One of the biggest promises of the Industrial Internet of Things is to make use of real-world data gathered through wireless sensor networks (WSNs) to drive higher efficiencies and to streamline business practices. The demands on WSNs are diverse, with sensors placed throughout buildings, city streets, industrial plants, tunnels and bridges, moving vehicles or in remote locations such as along pipelines and weather stations. A common requirement across such applications for the Industrial Internet of Things is for WSNs to deliver both low power and wire-like reliability and to do so across a broad spectrum of network shapes, sizes and data rates.

Wireless mesh networks have become increasingly well accepted due to their ability to cover large areas using relatively low power radios that relay messages from node to node and to maintain high reliability by using alternate pathways and channels to overcome interference. One technique in particular, called Time Synchronised Channel Hopping (TSCH) mesh networking, pioneered by Linear Technology's Dust Networks and incorporated into the WirelessHART industrial standard, is field proven to deliver the performance needed by the Industrial Internet of Things. TSCH networks typically experience better than 99.999% data reliability and all wireless nodes, even routing ones, enjoy multi-year battery life on small lithium batteries.

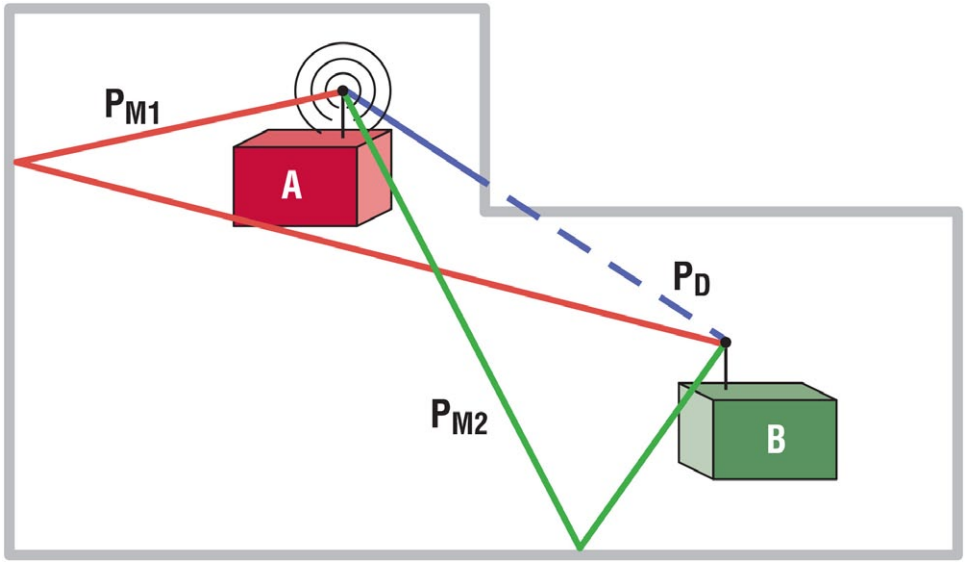

Figure 1. *Multipath fading – A radio signal's strength at the receiver (B) is affected not only by the direct path (Pd), but also by reflections (Pm1 & Pm2) which may arrive out of phase and cause significant fading.*

However, a variety of mesh networks use similar sounding networking techniques (e.g., "frequency agility" vs "channel hopping," "sleepy" vs "time synchronised" meshes), and yet yield drastically different performance levels. These wireless networking details determine how such protocol level choices greatly impact a WSN's performance and the network's overall suitability for an application.

Wireless sensor network challenges

Since wireless is unreliable by nature, it is important to understand the sources of unreliability to be able to account for them in a communications system. Unlike wired communications, where the communications signal is shielded from the outside world by cabling, RF propagates in the open air and interacts with the surrounding environment. There is the possibility for other RF transmission sources causing active interference.

However, much more common is the effect of multipath fading, where the RF message may

be attenuated by its own signal reflected off of surrounding surfaces and arriving out of phase (Figure 1). The effects of multipath change over time, as nearby reflective surfaces (e.g., people, cars, doors) typically move. The net result is that any one RF channel will experience significant variation in signal quality over time.

Further adding to the challenge is the fact that multipath fading is unpredictable. By definition, a network must be actively transmitting on a channel to experience (and therefore measure) the channel's performance in the face of multipath fading. Therefore, while the notion of using a simple passive signal strength measurement (RSSI) of an unused channel may be helpful to detect active interferers, it cannot predict that channel's suitability in the face of multipath fading.

Fortunately, since multipath fading affects each RF channel differently and changes over time, using channel hopping for frequency diversity minimises the negative effects of multipath fading. The challenge for WSN protocols is the ability to use channel hopping over large networks with multiple hops.

Common approaches seen in WSNs

Understanding how different WSNs perform in the face of these constraints (see the full version of this article, click below for the download) is assisted by examining techniques often used in some wireless mesh networks to address frequency diversity and to deliver low power. These can include; Single channel WSNs and channel agility; and Duty cycling by network-wide sleeping, in various forms. We can then consider the properties of Time synchronised channel hopping mesh networks, and the features and resilience that are enabled by that approach.

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BEAM-FORMING ANTENNAS: ESSENTIAL TO THE NEXT PHASE OF MOBILE NETWORK GROWTH

By Victor Fernandez, Anritsu

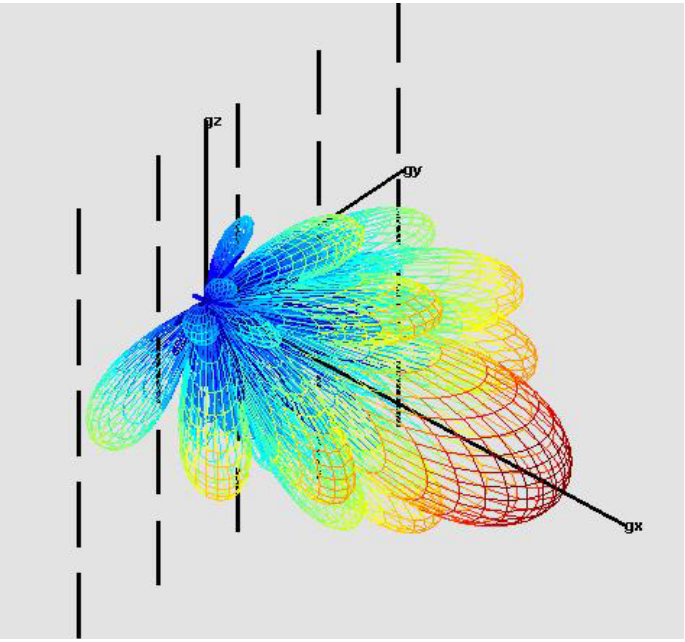
Before 2014, LTE technology deployments worldwide were principally of the frequency division (FD-LTE) variety. It was only in 2014 that the other, time division (TD-LTE) flavour of LTE began to gain serious attention from the mobile telephone industry.

One of the main benefits of TD-LTE is its ability to support the use of beam-forming (that is, highly directional) transmitting antennas. Beam-forming antennas offer network operators important benefits, enabling a more flexible and efficient use of network infrastructure and, in some circumstances, a markedly better quality of service to customers.

This means that both manufacturers and users of antennas and base transmitter station (BTS) equipment are currently exploring new approaches to the design, production, installation and use of beam-forming antennas. This article outlines methods engineers may use to design and build beam-forming antenna prototypes, and the role that specialised RF measurement instrumentation can play in the evaluation of such prototypes.

Comparison of multi-antenna operating modes

The radio access technologies used in modern communications networks rely to a large extent on various multi-antenna systems to achieve high data rates or to improve the quality of transmission to users at the perimeter of a cell. These multi-antenna systems may be of the multiple-input, multiple-output (MIMO) type, single-input, multiple-output (SIMO) or multiple-input, single-output (MISO).



In a BTS, a multi-antenna system may be used to transmit signals by one of two opposing and clearly differentiated techniques. These techniques are commonly confused.

One use of multiple antennas is to transmit a different data stream through each antenna. This is possible when there is a low degree of correlation between the different transmission paths, for instance because the transmitter is in an environment which tends to scatter RF transmissions, causing each data stream to attempt a different path to the receiver. In this case, the receiver sees each antenna as an independent signal source, and readily distinguishes the different data streams. The effect is to increase the overall data rate. This technique is called spatial multiplexing.

The other use of a multi-antenna system is possible when all the transmission paths are closely correlated, and every signal is affected by the transmission medium in a similar way – for example in an environment subject to negligible scattering, or when the antennas are mounted close to each other. In this case, the multiple antennas can operate as though they were a single, high-power antenna with its main

lobe illuminating a specific area.

When an antenna array is used in this way, it is a beam-forming antenna. The effect is to concentrate the available bandwidth in the targeted area, improving the quality of transmission or the signal-to-interference-plus-noise ratio (SINR).

FD-LTE can employ multi-antenna systems for spatial multiplexing very effectively, since the multiple-carrier waveforms it uses, such as orthogonal frequency division multiplexing (OFDM), can be perfectly matched to this kind of transmission system architecture.

TD-LTE, on the other hand, can make particularly good use of beam-forming antennas, as the uplink and downlink are duplexed in the time domain and, more important, transmitted and received signals are at the same frequency.

Beam-forming antenna technology, then, is important to the deployment of today's TD-LTE technology, but it is also expected to play an important part in 5G network infrastructure, which will combine enhancements to LTE with new radio access technologies. This is because of the requirement to support 'network densification'– that is, the deployment of small cells with a single carrier waveform to serve small areas packed simultaneously with many subscribers. This will be achieved through the implementation of so called 'massive MIMO' beam-forming techniques.

Techniques for realising a beam-forming antenna

A beam-forming antenna may be realised either mechanically or electronically.

The mechanical method requires the physical manipulation of the antennas to adjust their position and orientation, in order to ensure that all their transmissions are in phase or highly correlated in relation to the target area. While easy enough to understand, its implementation is impracticable in the field, because of the need to frequently and precisely change the position and direction of the beam as user equipment or sources of interference move. Moreover, the mechanical method requires the use of antennas with an extremely precise radiation pattern characterised by a narrow main lobe, in order to clearly focus their RF output and enable a quick estimation of each required mechanical movement.

Fortunately, the same beam-forming operation can be implemented electronically, using static antennas. Electronic control of an antenna array's radiation pattern is possible because two or more identical antennas may be configured in such a way that they behave as one single equivalent antenna with a known radiation pattern.

This radiation pattern depends on the type of antenna being used in each element of the array, the position of each element relative to the other elements, and the amplitude and phase of the signal fed to each one. This enables 'smart' antennas to modify their radiation pattern in response to an internal feedback loop while the antenna system is operating. This ability to dynamically alter the direction and shape of an antenna's beam offers great advantages to network operators, improving the efficiency and flexibility of a wireless communication system.

In the continuation of this article, the author expands on the basic design parameters of a smart beam-forming antenna, and shows how – with only a suitable 2-channel signal generator – it is possible to experiment with the fundamentals of beam-forming on the lab bench. Click below for download.

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DESIGNING ROBUST, FULLY ISOLATED (DATA & POWER) I²C/PMBUS DATA INTERFACES

BY MAURICE O'BRIEN

A key requirement for industrial and instrumentation (I&I), telecommunications, and medical applications is a reliable interface for transmitting data. The Inter-Integrated Circuit (I²C) bus is a 2-wire bidirectional bus used for low-speed, short-distance communication between integrated circuits. The Power Management Bus (PMBus), a relatively slow 2-wire communications protocol based on I²C, is targeted at digital management of power supplies. The PMBus protocol defines an open-standard digital power management protocol that facilitates communication with a power converter or other connected device. Examples of isolated I²C applications include:

- Isolated I²C, SMBus, or PMBus interfaces
- Level-translating I²C interfaces for power supplies
- Networking and Central office switching
- Power-over-Ethernet
- Telecommunication and data communication equipment
- Isolated data acquisition systems
- –48 V distributed power systems and modules

Dual I2C isolators with DC/DC

The figure compares PMBus isolation using discrete components with a fully integrated solution. The discrete approach requires four optocouplers for isolation, an isolated power supply, and complex analog circuits to prevent latch-up and suppress glitches. The isolated power supply uses a transformer driver IC to drive a discrete transformer, along with a simple rectifier and low-dropout regulator to clean up the isolated rail. This design requires eight ICs and several passive components, and burdens the interface with higher cost, increased PC board area, and lower reliability.

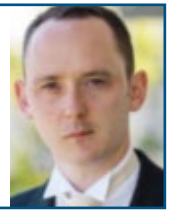
The integrated solution (ADM3260) provides a fully isolated bidirectional I2C interface and isolated power with a single IC, plus the decoupling capacitors and pull-up resistors associated with any I²C interface. The ADM3260 is free of glitch and lock-up issues, has UL approved 2.5 kV rms isolation ratings, and is offered in a 20-lead SSOP package. It provides bidirectional isolated data and clock lines and isolated power without the size, cost, and complexity of optocouplers.

This single-chip solution significantly reduces the cost, design time, and PC board area required for an isolated I²C interface, while enhancing reliability. It operates from 3.3-V or 5-V supplies without modification, avoiding the design changes that would be necessary with a discrete design, and provides 150 mW of output power at 5 V or 65 mW at 3.3 V, allowing it to power ADCs, DACs, or other small systems on the isolated side.

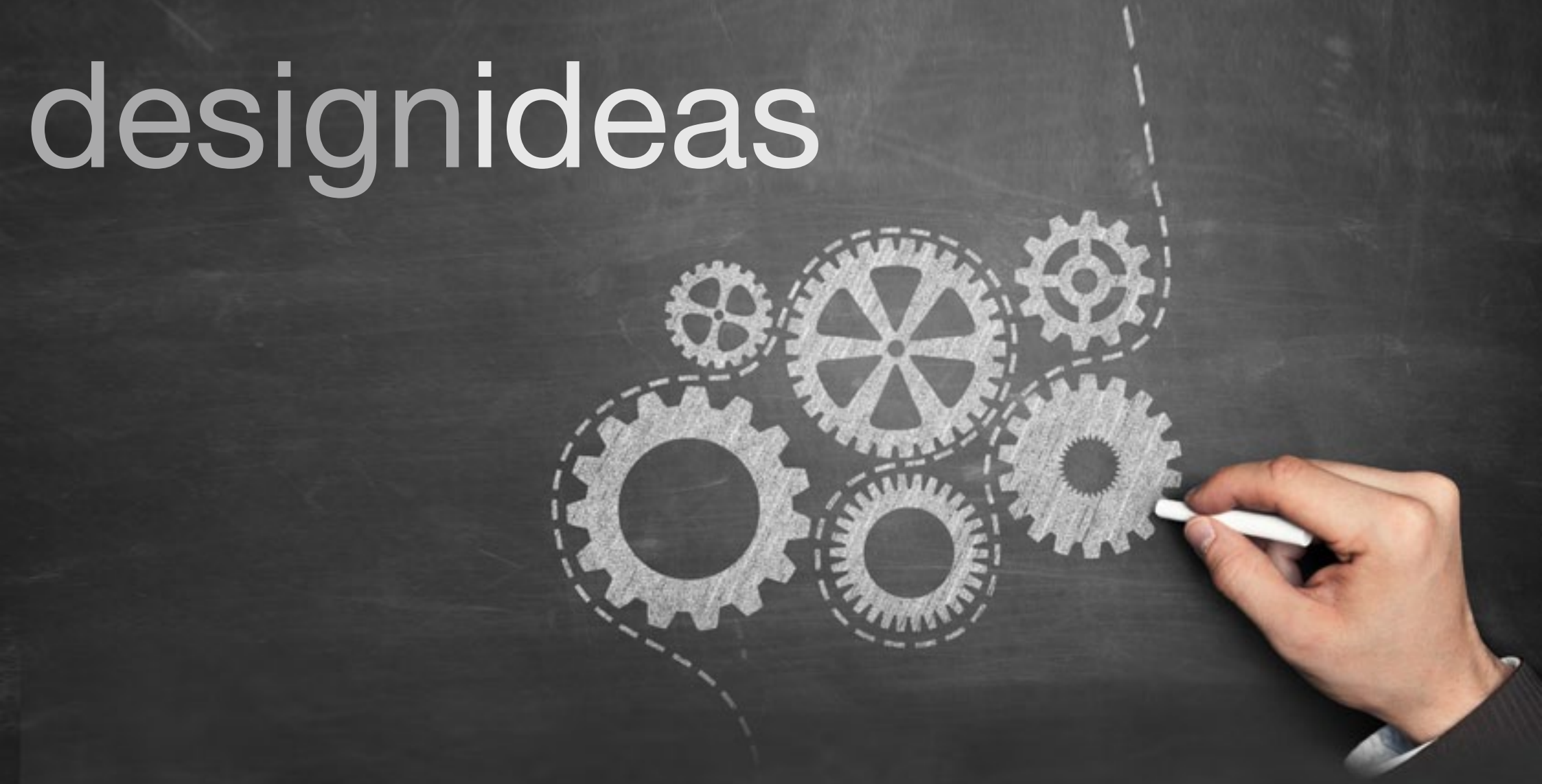
Conclusion

Isolated I²C/PMBus links in industrial and instrumentation, telecommunications, and medical applications need to be small, robust, and inexpensive. By integrating chip-scale transformer isolation, a single-chip can implement a fully isolated I²C/PMBus data link including isolated power. The ADM3260 hot swappable, dual I²C isolator with integrated dc-to-dc converter can provide a compact, reliable, low-cost, high-performance solution for these demanding applications while significantly reducing circuit complexity and design time.

Maurice O'Brien *[maurice.obrien@analog.com] joined Analog Devices in 2002, following his graduation from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. He currently works as a product marketing manager in the Power Management product line. In his spare time, Maurice enjoys horse riding, outdoor sports, and travel*



designideas



- Circuit gates pulse train without truncating
- Circuit lets AGC amp hold its gain
- Linear ramp generator uses one op-amp

Circuit gates pulse train without truncating

By Viktor Safronov

To gate an integral clock pulse sequence from a continuous source without distorting pulse duration and number is not a trivial task. In most cases, a simple AND gate will cause problems, see Figure 1.
Clock pulses pass through the AND gate as long as the asynchronous strobe E is high. If loss or distortion of even one pulse is critical, then the simple AND gate is unsuitable, as the first and the last pulse in the burst will often be distorted (shorter than usual pulse) due to the lack of synchronisation between clock and E.

This Design Idea demonstrates a mathematical approach to synthesise an asynchronous gated circuit able to gate an accurate pulse train from a clock signal without distorting pulse duration. Such circuits are called quantisers (Figure 1).

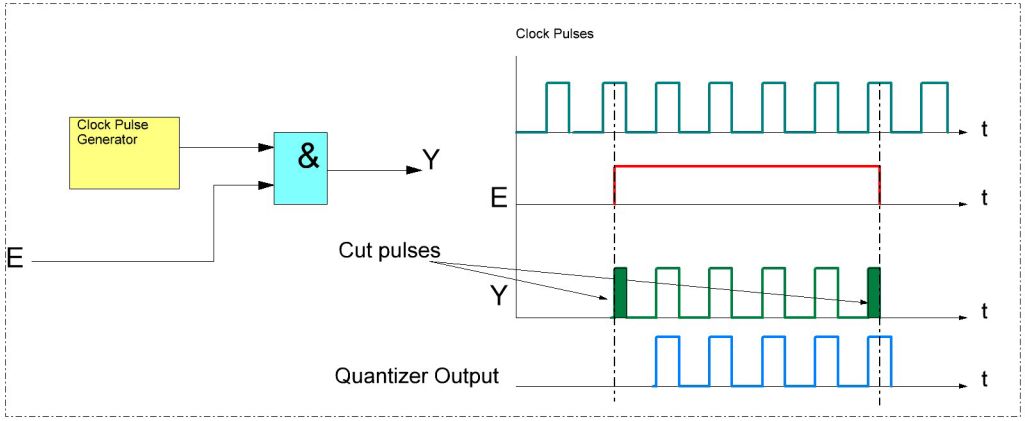


Figure 1. *Two ways of gating pulse train, using gate signal E and an AND gate (Y output), or a quantiser (blue)*

Output \ G	E		
1	①0	2	-	3
2	1	②0	5	-
3	1	-	4	③0
4	-	2	④0	3
5	-	6	⑤1	7
6	1	⑥0	5	-
7	1	-	5	⑦1

Figure 2. *Asynchronous finite-state machine (FSM) transition primary table, where 1,2,3,4,5,6,7, the numbers of stable FSM states, are circled (G is the clock input)*

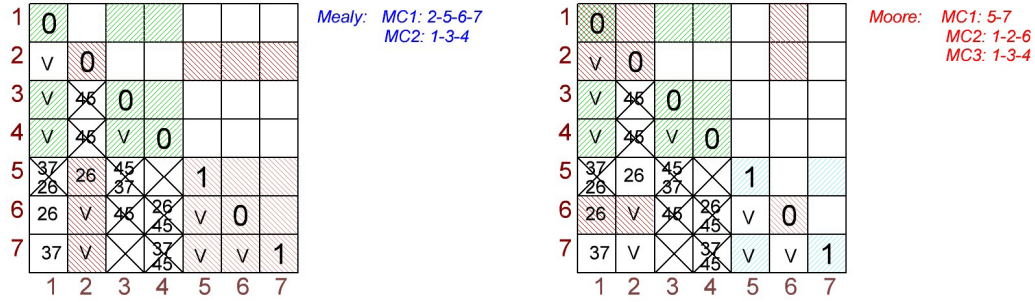


Figure 3. *Final pairs tables by Mealy (left) and Moore (right), where:*
- MC1: 2-5-6-7 and MC2: 1-3-4 are maximum compatible sets (by Mealy)
- MC1: 5-7, MC2: 1-2-6 and MC3: 1-3-4 are maximum compatible sets (by Moore)

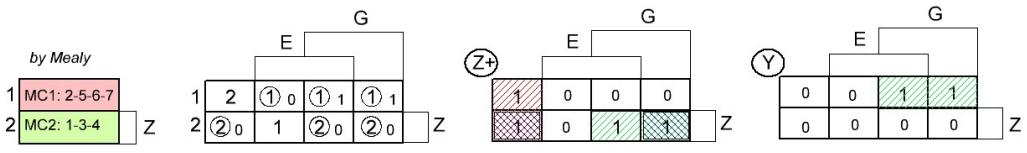


Figure 4. *Map of Z-coding (by Mealy), compressed state transition table, and Z-Y Karnaugh-Veitch maps*

Let's make a state transition table based on the operational principle of a quantiser (Figure 2).
Using Figure 2, let's make final pairs tables according to Mealy and Moore (Figure 3).

As we can see from Figure 3, total coverage by Moore requires a greater number of maximum compliant subsets, i.e., it's worse. On the other hand, the first state is alternatively a part of sets MC2 and MC3, which presents opportunities for extra circuit optimisation. However, we shall not consider this further.

Now, it's easy to draw a compressed state transition table and Karnaugh-Veitch maps for the Z-coding memory element and output gated signal Y (Figure 4).

Bearing in mind the Karnaugh-Veitch maps, let's write down logic equations for the synthesized circuit:

$$z^{+} = \overline{G}\cdot\overline{E} + G\cdot z + \overline{E}\cdot z = \overline{E}\cdot(\overline{G}+z) + G\cdot z = \overline{\overline{E}\cdot G\cdot z\cdot \overline{G}\cdot z} \quad \& \quad y = G\cdot\overline{z}$$

The minterm [/E · z] for z+ in this formula is not redundant as it may seem. It plays the important role of a counter-race bridge between minterms [/G · /E] and [G · z], eliminating their consecutive races at all edges of G.

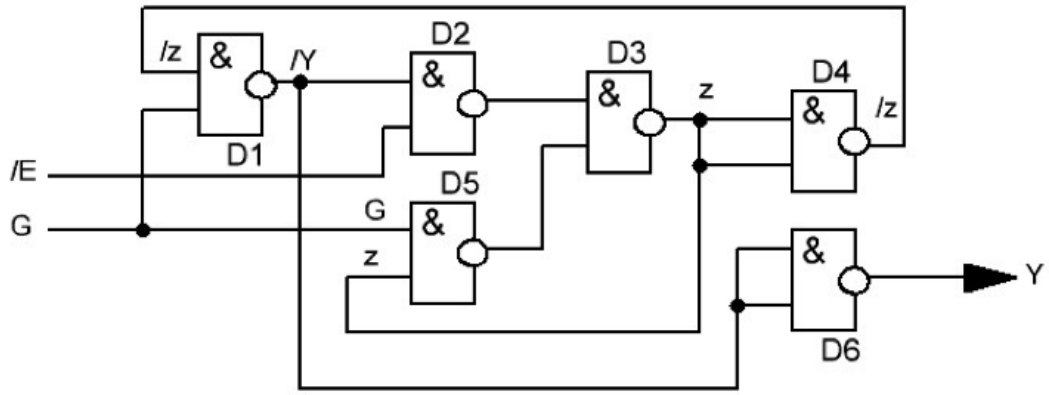


Figure 5. *Example implementation of the quantizer, where:*
- /E = inverted input of the asynchronous strobe signal
- G = clock
– Y = quantiser output

It is possible to add some extra features – for example, FLAG. When FLAG is low, the first pulse in the burst is not cut, but incorporated in the burst without affecting its duration. When FLAG is high, the first pulse is cut and excluded from the burst. The state of the FLAG should be kept unchanged until the next strobe pulse, so your equipment has enough time to read it and use for further processing.

This type of quantiser may be useful in designs sensitive not only to the number of pulses in the burst, but to the pulse phase; for example, in radar equipment.

Circuit lets AGC amp hold its gain

By Vladimir Rentyuk

AGC (automatic gain control) amplifiers are frequently-used devices. Their gain is a function of the level of their input signal. The main function of AGC amplifiers is compression of a signal, but sometimes the gain needs to be temporarily frozen. This Design Idea provides just this function.

Let's examine this idea with Analog Devices' SSM2166 as an example. The SSM2166 is a microphone preamplifier with variable compression and noise gating whose transfer characteristics are in Figure 1 and typical application diagram in Figure 2.

The chip has one interesting feature which isn't presented in the data sheet: we can control the gain using an external voltage applied to pin 8 (AVG CAP). Table 1 shows the observed level detector voltage (pin 8) vs. input voltage. A simple circuit which provides gain-hold capability to the SSM2166 by fixing the output voltage of the internal level detector is shown in Figure 3. Auto-tracking of the voltage level on the AVG CAP is done by sample-and-hold amplifier IC1 (LF398). This level is duplicated on Hold CAP if IC1.8 is high – the SSM2166 is working in compression mode. When you want to hold the gain, drive this pin low. IC1 will then hold the voltage level on Hold CAP, and analogue switch IC2 (ADG417) will connect IC1's output to pin 8 of the SSM2166, overriding the level detector.

Input dB	Level detector VDC
0	4,00
-10	3,56
-20	2,88
-30	2,28
-40	1,80
-50	1,41
-60	1,00
-70	0,60

Table 1. *Level detector voltage (pin 8) vs. input voltage (observed dependence)*

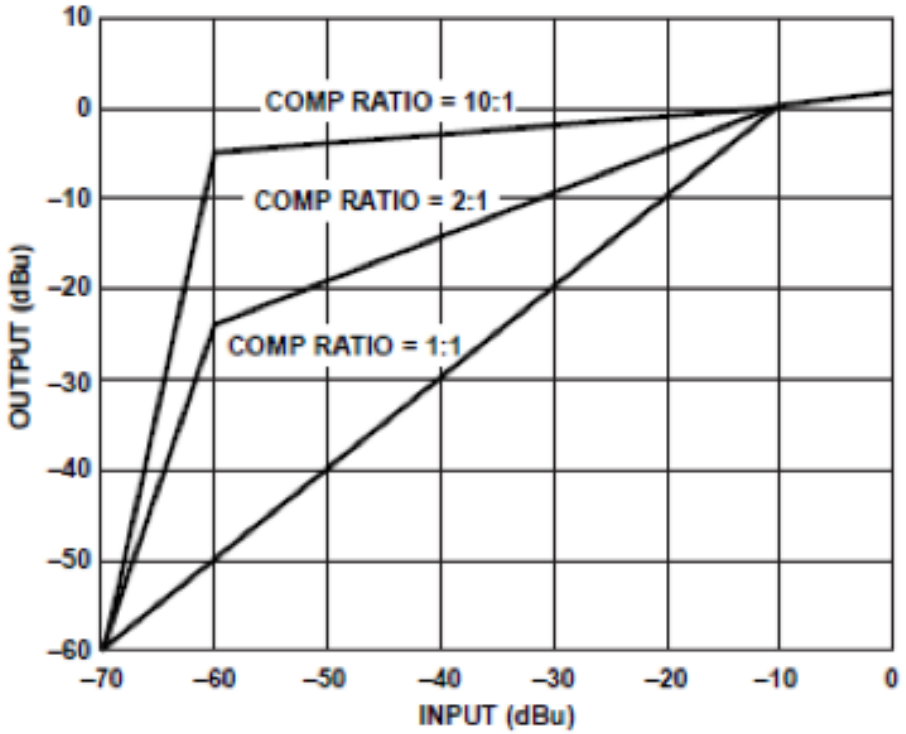


Figure 1. *Compression and gating characteristics with 10dB of fixed gain*

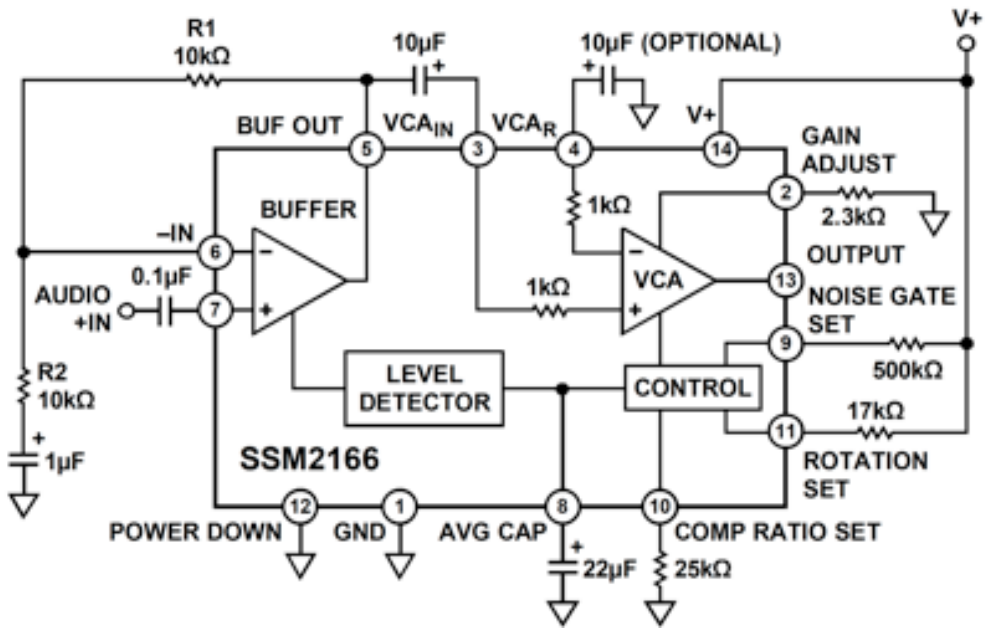


Figure 2. *SSM2166 functional block diagram & application circuit*

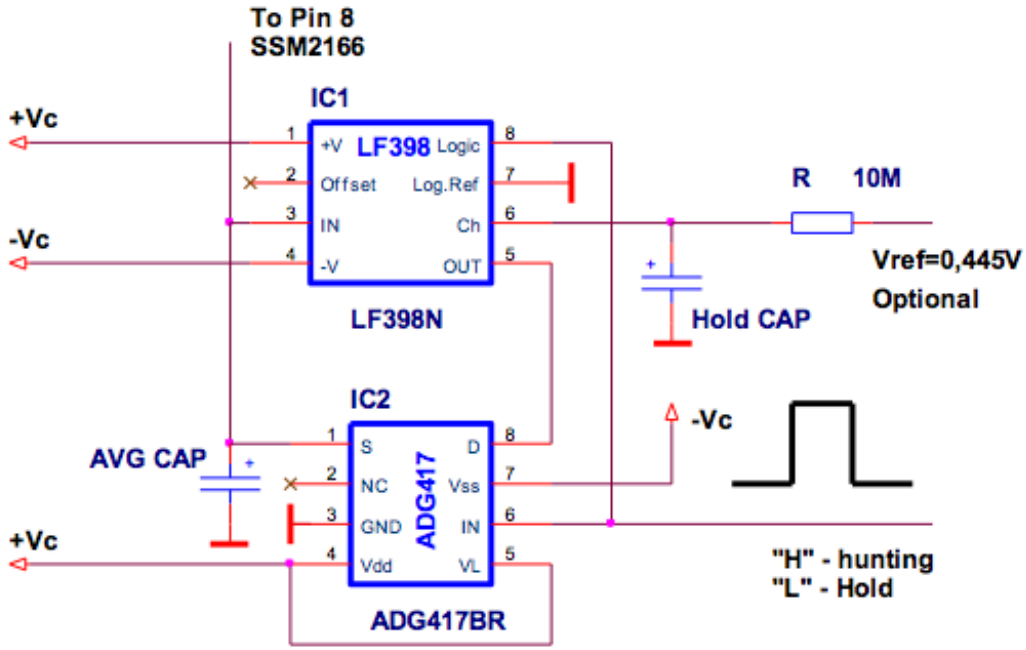


Figure 3. *Circuit provides hunting and holding gains for SSM2166*

This Design Idea works with other types of AGC amplifiers, too [Ref.]. But in this case, an analogue switch is unnecessary. In these circuits, a sample-and-hold amplifier should be connected between the level detector and voltage controlled attenuator.

Reference

Rentyuk, Vladimir "Use of an AGC Amplifier as a Soft Limiter of Signals", Electronics World, May 2010

About the author

Vladimir Rentyuk graduated from Zaporizhzhya Machine Construction Institute (Ukraine) in 1978, earning the equivalent of a master's degree in radio engineering and has worked at the Zaporizhzhya Research Institute of Radio Communication, ZSE Radiopribor, and, since 2002, as a development engineer at Modul-98 Ltd., developer of embedded electronic systems, robotic equipment and image recognition systems. His areas of expertise include analogue design techniques, computer simulations and writing of technical articles that have been published in the US, UK, Russia and Ukraine.

Linear ramp generator uses one op-amp

By Einar Abell

This Design Idea demonstrates a simple way to turn a step input into a ramp of nearly constant slew rate. The basic circuit uses a single op-amp; a circuit built on an integrator will typically require three. Figure 1 shows the basic circuit.

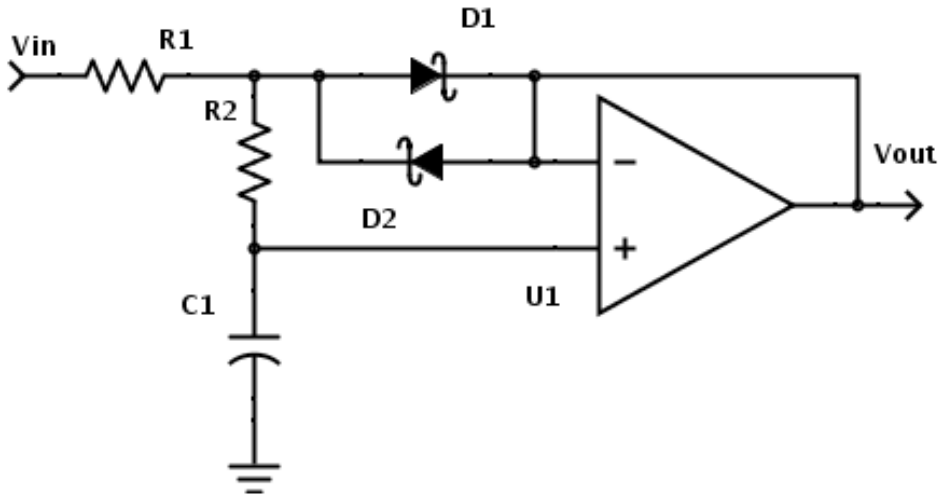


Figure 1. *Ramp generator*

The op-amp is wired as a voltage follower, with D1 & D2 clamping the input to one diode drop above or below the output. When the input step-changes by a volt or more, the diodes will keep the voltage across R2 at a nearly constant 0.3V (because the output will follow any change on C), creating a constant slew rate at the output of 0.3V/R2C1 V/s. The output will slew to within 0.3V of the input and then follow an RC ((R1+R2)C1) curve until reaching a final value equal to Vin. For best results, R2 should be larger than R1, preferably by factor of ten or more. This simple circuit gives best results with fairly large steps, where the slow settling time won't be objectionable.

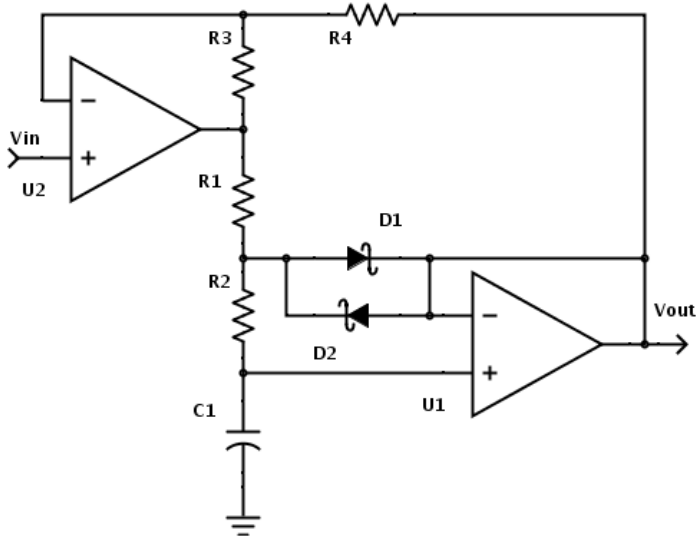


Figure 2. *Improved ramp generator*

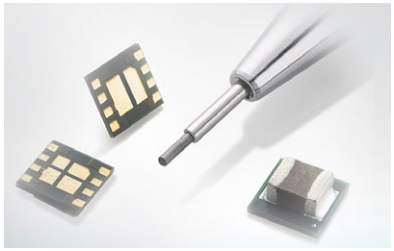
Figure 2 adds an extra amplifier to make the output slew to within a few millivolts of the input. Amplifier U2 amplifies the difference between the input and the output so as to keep the diode clamp operating until the output voltage nearly reaches the input. The output will slew to within the diode forward voltage divided by the gain of U2 (that is, 1+(R3/R4)). If the gain is made too large, the circuit will become unstable. The slew rate of U2 should be at least ten times (the higher the better) the output slew rate times the gain of U2. U2 needs extra headroom to keep D1 & D2 conducting, which usually means restricting the input so that it is more than one volt away from the max/min output swing of U2.


productroundup
SL871
Telit
TOSHIBA
TPHR8504PL
MOSFET
5.0mm
IOR
07BFA6
EXAR
XRP9710
XRP9711
efus
Linux
TOSHIBA
TB67H303HG
econais
EC19D
lesswire
WiBear 11ac
ROHM
SEMICONDUCTOR
LINEAR
TECHNOLOGY
LT8490
MICROCHIP
dsPIC33EP128GM304
DIODES
AP7340
IOR

productroundup

TI grows “nano power” DC/DC module range

Additions to Texas Instruments’ Simple Switcher nano modules will, says TI, “redefine small power supply design” - they are positioned as the smallest-available, high-efficiency 17V and 5V (input) DC/DC power converter blocks that deliver currents in the 100-mA to 2-A range. The 17-V, 0.65-A LMZ21700 and 1-A LMZ21701, as well as the 5-V, 1-A LMZ20501 and 2-A LMZ20502 DC/DC power modules are chip-scale packages with a surface-mount inductor mounted on top; completing the DC/DC function typically requires only the addition of chip capacitors. The modules, TI says, offer an overall solution size that is up to 40% smaller than a discrete implementation.



Complete article, here

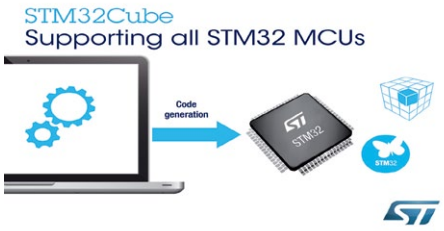
Dimmable lighting-LED chip simplifies driver designs

Dialog’s MR16-lamp dimmable led driver, the iW3662, uses digital control to optimise compatibility with virtually any transformer (electronic or magnetic), to loads as low as 4W; the LED driver is designed to solve transformer and dimmer compatibility issues in low-voltage lighting applications. The greatest challenge in designing low-voltage MR16 LED retrofit bulbs, Dialog asserts, is the installed base of AC step-down electronic transformers. The iW3662 LED uses digital analytics to detect installed electronic transformers and dynamically increases the peak loading to latch the transformer.

Complete article, here

Single coding platform for all STM32 (ARM) MCUs

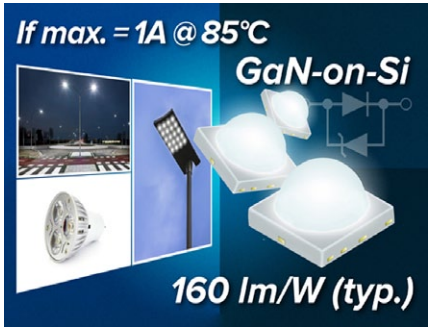
Designers targeting any of STMicroelectronics’ STM32 microcontrollers can now make use of the STMCube software development platform. STM32Cube enables a quick start with any STM32 device and simplifies porting of code from one product series to another. The development platform is available for all devices in volume production, from the ultra-low-power to the very-high-performance series. The platform comprises the STM32CubeMX graphical configurator and initialisation C-code generator, which provides wizards that help configure the pin-out, clock-tree, and peripherals, and meet constraints on power consumption.



Complete article, here

GaN-on-Si white LEDs deliver more light

Toshiba’s latest high-luminous-efficacy white LEDs output luminous flux exceeding 160 lm. This series of high power LEDs is suitable for use in residential, commercial and industrial lighting applications, delivering high luminous flux at room temperature operation. Under conditions of Ta = 85°C, operating current can be driven to 1A and luminous flux is more than 60% greater than that offered by the preceding TL1L3 series. Available in nine colour variations from 2700K to 6500K, the TL1L4 series is built with gallium nitride-on-silicon (GaN-on-Si) wafer technology in a 3.5 x 3.5 mm lens package.

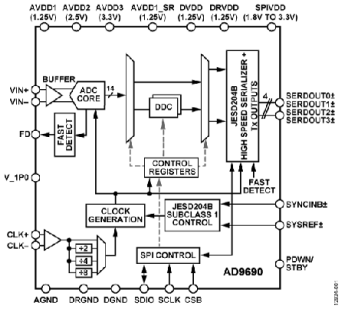


Complete article, here

productroundup

14-bit, 500 MSPS / 1 GSPS JESD204B, ADC

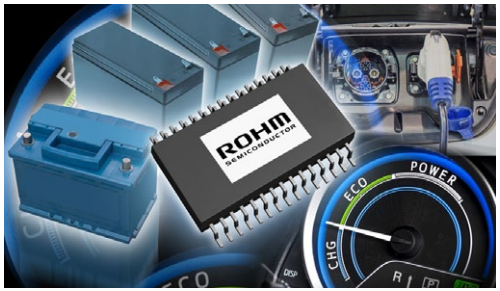
AD9690 is a 14-bit, 1 Gsample/sec analogue-to-digital converter, designed for sampling wide bandwidth analogue signals of up to 2 GHz. The AD9690 is optimised for wide input bandwidth, high sampling rate, linearity, and low power in a small package. The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations and the device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use.



Complete article, here

Monolithic EDLC ("supercapacitor") cell balancing IC

From Rohm Semiconductor, a cell balancing IC contributes to increased miniaturisation, greater stability, and longer life for EDLCs (electric double layer capacitors). BD14000EFV-C integrates over 20 discrete components required for EDLC cell balancing on a single chip, reducing mounting area by 38% over conventional solutions while eliminating component variations, simplifying configuration of compact, high reliability EDLC systems. In addition to cell balancing functionality for up to six cells, multiple ICs can be connected in series to enable simultaneous control of even more cells.



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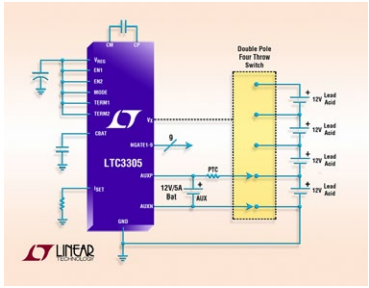
"New class" of 650V IGBTs cuts losses up to 20 kHz

Infineon Technologies has a new class of low saturation voltage (VCE(sat)) IGBTs specifically optimised for low switching frequencies ranging from 50Hz to 20 kHz. The devices have a breakdown voltage (V_{BR}) rating of 650V. With a typical $V_{CE(sat)}$ value at 25°C of 1.05V, new levels of efficiency can be reached – up to 0.1% efficiency improvement in a NPC 1 topology or up to 0.3% efficiency improvement in a NPC 2 topology when replacing predecessor TRENCHSTOP IGBTs with the L5 family. Coupled with the positive temperature coefficient of $V_{CE(sat)}$, high efficiency is maintained plus paralleling is straightforward.

Complete article, here

Lead-acid 48V battery-balancing IC

LTC3305 is a single-IC, stand-alone multicell battery balancer for 12V lead acid batteries. Charge is transferred using a lower capacity battery that is sequentially connected across the 4 batteries in the stack. Not only does this battery transfer charge, but the energy in the transfer battery adds to the total energy in the stack, thus increasing capacity. Included on the chip is sequencing, drive circuitry for high voltage external NFETs, voltage monitoring and protection. The LTC3305 is designed for stand-alone operation and does not require a microprocessor or other control circuitry. One battery in the stack can be replaced and quickly balanced to the remaining batteries.

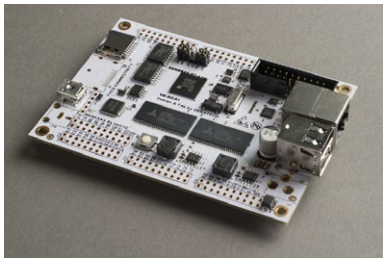


Complete article, here

productroundup

Development board hosts Renesas ARM Cortex-A9 core

Distributor Rutronik has Vekatech's VK-RZ/A1H development board which carries the RZ/A1H embedded microprocessor from Renesas, an ARM Cortex-A9-based MCU. The embedded microprocessor runs at up to 400MHz clock speed; integrates up to 10 MB of on-chip RAM, and has an OpenVG compatible graphics accelerator, dual LCD-drivers and camera inputs. The internal SRAM can hold two layers of WXGA size images making external SRAM redundant. Using serial QSPI-flashes enables compact HW-designs with low pin count ICs. The processor has 2x32 MB SDRAM and 2x8 MB QSPI-flash. Debugging can be performed via standard J-TAG connector.



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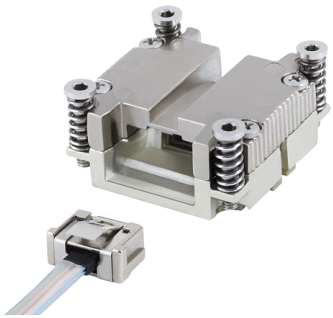
25 Gbit/sec optical on-board-transceiver

FCI's Leap On-Board-Transceiver (OBT) system is a one inch square, (2.5 x 2.5 cm) board-mounted optical module that features 12-transmit and 12-receive channels, each working at 25 Gbit/sec over distances up to 100m with a total of 300 Gbit/sec throughput. The OBT is designed to be placed near a host ASIC which results in shorter copper board traces, better signal integrity and lower power consumption. The transceiver is connected to the board via an FCI proprietary surface mount electrical BGA/LGA socket. Optical connectivity to-and-from the OBT is realised by using a high-density ribbon fibre assembly.



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Code configuration plug-in for 16-bit PICs

The MPLAB Code Configurator for Microchip Technology's MPLAB X IDE speeds and simplifies development of firmware on 8- and 16-bit PIC MCUs, to more easily develop device initialisation and implement peripheral drivers. This expansion of the MPLAB Code Configurator Plug-In supports 16-bit PIC MCUs, in addition to the 8-bit devices already supported. The Code Configurator is a free plug-in tool with a GUI for controlling and driving the peripherals inside PICs with simple and clearly documented driver APIs, and now includes support for PIC24 families. It is easy to change peripheral configurations or add/remove peripherals from your project. Once a system-level clock rate is set, the tool will automatically calculate timer periods, duty cycles and baud rates for peripherals. With a drag-and-drop style interface, this tool generates easy-to-read code that includes peripheral configuration setup, drivers and pin mapping to efficiently solve application development obstacles.

Complete article, here

Low resistance power FETs in smaller packages

TI's NexFET n-channel power MOSFETs claim the lowest-available on-resistance, for 25-V and 30-V devices in 5 x 6 mm QFN packages. 11 n-channel power MOSFETs join the NexFET product line for hot-swap and ORing applications with the lowest on-resistance (RDS(on)) in a QFN package. In a separate range, TI's 12-V FemtoFET CSD13383F4 for low-voltage battery-powered applications achieves the lowest resistance at 84% below competitive devices in a 0.6 x 1 mm package. The 25-V CSD16570Q5B achieves a maximum of 0.59 mΩ of RDS(on), while the 30-V CSD17570Q5B achieves a maximum of 0.69 mΩ of RDS(on).

Complete article, here

productroundup

Safety-critical code verification extended for C++

PRQA has added functionality in its latest releases of its QA·C and QA·C++ static analysis tools, including Dataflow, Graphical and Command Line Interfaces, support for Modern C++ features and improved coverage for MISRA C++ and HIC++. Specific upgrades include; Dataflow analysis, enhanced Graphical and Command Line Interfaces, support for the latest Modern C++ language features, and an improved level of coverage for compliance with the MISRA C++ and High Integrity C++ (HIC++) coding standards. The Dataflow engine in both QA·C++ and QA·C can now perform pointer alias modelling on class and structure pointer members. The internal representation of class/structure members has been changed to a form which can be processed more efficiently by the SMT Solver, boosting the speed, depth and accuracy of the analysis. Additional enhancements to the cross-platform architecture and updated Graphical and Command Line Interfaces include better integration to IDEs (MS Visual Studio and Eclipse).

Complete article, here

SiC MOSFET range extended at 1200V ratings

ST's SCT20N120 silicon-carbide power MOSFETs will, the company asserts, brings advanced efficiency and reliability to a broader range of energy-conscious applications. The 1200V SCT20N120 extends the family, with on-resistance (RDS(ON)) better than 290 mΩ up to the 200°C maximum operating junction temperature. Switching performance is also consistent over temperature thanks to highly stable turn-off energy (Eoff) and gate charge (Qg). The resulting low conduction and switching losses, combined with ultra-low leakage current, simplify thermal management and maximise reliability.

Complete article, here

5V, ARM Cortex-M4F MCUs for motor control

Toshiba's TMPM470FDFG and TMPM475FDFG enable dual control of two brushless DC motors; they are based around the ARM Cortex-M4F core and are in the TX04 series. TMPM475FDFG integrates a CAN (Controller Area Network) controller for use in factory automation systems. The processor core in both parts can operate at a clock speed of up to 120 MHz. They incorporate two modules, each containing a programmable motor drive, 12-bit AD converter and vector engine, ensuring the efficient and simultaneous operation of two brushless DC motors from a single chip. They have an operating voltage ranging from 4.5 to 5V.

Complete article, here

"Smart-lighting" manager energy-harvests daylight, with internet connections

ams' AS721x Autonomous Daylighting Manager is positioned as the first integrated chip-scale Internet of Things (IoT)-connected smart lighting manager, providing connected, integrated control capabilities to luminaire, light engine and replacement lamp manufacturers. Photopic sensors built with nano-optic filters integrated into the AS721x series are designed to help lighting manufacturers address the growing challenges of energy-saving lighting mandates, including daylighting controls. These challenges are more cost-effectively met by bringing the controls, connectivity, such as Bluetooth, and high-granularity sensing into the luminaires themselves. The AS721x Autonomous Daylighting Manager senses the ambient daylight and enables the delivery of constant lux levels in the space by managing subtle adjustments as the amount of outside light varies. The approach also delivers accurate lumen maintenance over time and temperature variation.

Complete article, here

ORIN LANEY

Fixing a mainframe with a lunch bag

Way back when I was an 18-year-old starving college student, a friend and fellow electronics enthusiast heard about summer jobs at an IBM datacenter. We leaped at the chance to score some cash inside a tech company and were duly hired as "supplemental customer engineers." This meant we worked with the regular CEs in maintaining mainframe systems, but we handled routine or dirty work while they took care of the brainy stuff.

I spent a lot of time making wire wrap changes, pulling cables under false floors, and similar tasks. The datacenter ran 24 hours per day. We were on the graveyard shift. This brought an interesting change of clientèle. If the daytime customers wore three piece suits and had impeccable haircuts, the night crowd wore jeans, pushed their mag tapes around in old shopping carts, and put their feet on the console.

One night I was alone in the CE room when a floor employee walked in looking for help. A System/360 Model 50 would not power up. Although I had experience working inside the various systems I had never received any training on the internals, let alone circuit details. Nevertheless I knew something about electronics and was confident that I could take a shot at it without doing damage, so why not give it a try? Every other CE was out at a customer site somewhere. It was me or nobody.

Daniel Vasconcellos

I headed to the errant machine and turned it on. There was a sound of relays clacking as the power supplies came up in a predetermined sequence. A few lights came on. Then the system paused, I could hear relays dropping out one by one, and the lights turned off.

The Model 50 schematic came in giant binders, many of them, on a rolling cart. Rummaging through the cart I found the master index and located the binder for power. After finding the appropriate page, I studied how the relays were interconnected and located them inside the cabinet. Then it was a matter of using a multimeter to test the first relay in the sequence, then the second, and so forth until I found the fault. I started cycling power, testing each relay in turn.

It was the fourth or fifth relay, I don't remember which, that turned out to be the problem. It actuated mechanically, but no power appeared on the output side of the contacts. Closer inspection showed that the contacts were blackened. Arcing on closure and release had eventually coated them with enough oxide to build up an insulating barrier. I had never before serviced a relay contact but I knew you were supposed to use something called a burnishing tool. I didn't have one.

Returning to the CE room to see what tools might be laying about, nothing resembling a burnishing tool could be found. Then I noticed a discarded lunch bag in a trash can. It was made from the stiff brown paper typical for sturdy bags, such as those for carrying groceries. The coarse wood fibres might serve as a sort of soft, gritless sandpaper. I tore off a strip and headed back to the Model 50. After inserting the paper between the dirty contacts I pressed the relay closed and pulled the paper through. It came out with a black streak on it. I repeated this until the tracks were clean and finished the other contacts. The moment of truth came when I powered the machine again and it came up in all its light-festooned glory. Looking back, I suppose that's not bad for a skinny summer hire with few tools and no training on the hardware.

Orin Laney *holds MSEE and MBA degrees and is a licensed PE and certified EMC engineer. He is an independent signal integrity and EMC consultant based in Silicon Valley, California. You can reach him here.*

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CONTACTS

PUBLISHER
André Rousselot
+32 27400053
andre.rousselot@eetimes.be

EDITOR-IN-CHIEF
Graham Prophet
+44 7733 457432
edn-editor@eetimes.be

Patrick Mannion
Brand Director EDN Worldwide

CIRCULATION & FINANCE
Luc Desimpel
luc.desimpel@eetimes.be

ADVERTISING PRODUCTION & REPRINTS
Lydia Gijsegom
lydia.gijsegom@eetimes.be

ART MANAGER
Jean-Paul Speliers

ACCOUNTING
Ricardo Pinto Ferreira

european business press

SALES CONTACTS

Europe

Daniel Cardon
France, Spain, Portugal
+33 688 27 06 35
cardon.d@gmail.com

Nadia Liefsoens
Belgium
+32-11-224 397
n.liefsoens@fivemedia.be

Nick Walker
UK, Ireland, Israel, The Netherlands
+44 (0) 1442 864191
nickjwalker@btinternet.com

Victoria & Norbert Hufmann
Germany, Austria, Eastern Europe
+49 911 93 97 64 42
sales@hufmann.info

Monika Ailinger
Switzerland
+41-41-850 4424
m.ailinger@marcomedia.ch

Andrea Rancati
Italy
+39-02-284 6716
info@silvera.it

Colm Barry & Jeff Draycott
Scandinavia
+46-40-41 41 78
jeff.draycott@womp-int.com
colm.barry@telia.com

USA & Canada

Todd A. Bria
West
+1 831 477 2075
tbria@globalmediasales.com

Jim Lees
PA, NJ & NY
+1-610-626 0540
jim@leesmedia.com

Steve Priessman
East, Midwest, South Central & Canada
+1-630-420 8744
steve@stevenpriessman.com

Lesley Harmoning
East, Midwest, South Central & Canada
+1-218.686.6438
lesleyharmoning@gmail.com

Asia

Keita Sato
Japan
+81-3-6824-9386
MIshida@mx.itmedia.co.jp

Grace Wu
Asian Sources Publications Asia
(886-2) 2712-6877
wug@globalsources.com

John Ng
Asian Sources Publications Asia
(86-755) 8828 – 2656
jng@globalsources.com